

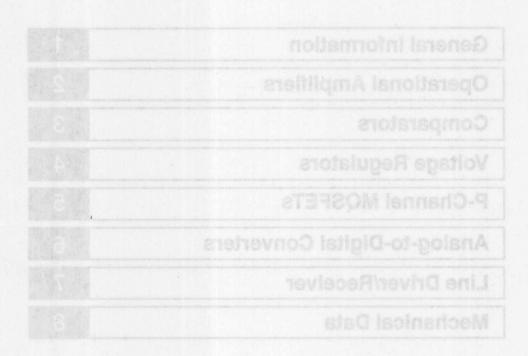
Linear Circuits 3-V Family

Data Book

1994

Linear Products

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Linear Circuits Data Book

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3-V Family

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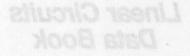
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INTRODUCTION

Texas Instruments offers the industry's first dedicated family of linear integrated circuits (ICs) that are specifically designed, characterized, and tested for operation at 3.3 V or less. This revised edition of the 3-V data book is expanded to include analog data converters and multichannel RS232 circuits, in addition to new offerings of operational amplifiers and comparators.

Many of the 3-V devices are available in the thin-scaled small-outline package (TSSOP), and all are available in the JEDEC-standard small-outline or through-hole packages. The TSSOP surface-mount package is just 1.1-mm (max) thick and can be a real space saver in densely packed designs.

While this manual offers information only on the 3-V analog devices available now from Texas Instruments, complete technical data for upcoming 3-V devices or any other TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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TLV2264A	2-3	3
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TLV23221	2-6	3
TLV2322Y	2-6	3
TLV2324I	2-8	7
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TLV2334I		•••
TLV2334Y		
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		~~
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	SM76LV4796
O-C	
8-8	TLV184SM
	TEV2217-3217-3217-3217-3217-3217-3217-3217-
	ASSSVIT
	YSUSSVIT
	TLV2264
	TLV2264A
	YL-928-LT
	ISSESUIT
	Vesesur
	TLV2224Y
	TLV2332I
	YISSAN
	YNESSAR
	TLV26/201
3-17	
	YSBECVIT
	TIV2254

operational amplifiers

DEVICE	VC		VIO (mV)	ICC (μA)	l _{IB} (pA)	CMRR (dB)	V <u>n</u> (nV/√Hz)	S/R (V/μs)	GBW (kHz)	DESCRIPTION		
	MIN	MAX	MAX	MAX	TYP	TYP	TYP	TYP	TYP	VO FORMAT INPUTS		
TLV2262	2.7	8	2.5	250	1	75	12	0.55	800	Dual, low noise, micropower, rail-to-rail		
TLV2262A	2.7	8	0.95	250	1	77	12	0.55	800	Dual, precision, low noise, micropower, rail-to-rail		
TLV2264	2.7	8	2.5	250	1	75	12	0.55	800	Quad, low noise, micropower, rail-to-rail		
TLV2264A	2.7	8	0.95	250	. 1	77	12	0.55	800	Dual, precision, low noise, micropower, rail-to-ra		
TLV2322	2	8	9	17	0.6	88	68	0.02	27	Quad, micropower		
TLV2332	2	8	9	250	0.6	92	32	0.38	300	Dual, low power		
TLV2342	2	8	9	1500	0.6	78	25	2.1	790	Dual, high speed		
TLV2324	2	8	10	17	0.6	88	68	0.02	27	Quad, micropower		
TLV2334	2	8	10	250	0.6	92	32	0.38	300	Quad, low power		
TLV2344	2	8	10	1500	0.6	78	25	2.1	790	Quad, high speed		
TLV2341	2	8	8	1500	0.6	78	25	2.1	790	Single, programmable power (high bias)		
TLV2341	2	8	8	250	0.6	92	32	0.38	300	Single, programmable power (medium bias)		
TLV2341	2	8	8	17	0.6	88	68	0.02	27	Single, programmable power (low bias)		
TLV2362	±1	±2.5	6	2250	2000	75	9	2.5	6000	Dual, low noise, high-speed		

comparators

DEVICE	V _{CC} (V)		VIO (mV)	Icc (μA)	IIB (nA)	IOL (mA)	^t pd (ns)	DESCRIPTION
	MIN	MAX	MAX	MAX	TYP	MIN	TYP	
TLV1393	2	7	5	125	40	0.5	650	Dual, low power
TLV2352	2	8	5	125	0.005	6	640	Dual, general purpose
TLV2254	2	8	5	250	0.005	6	640	Quad, general purpose
TLV2393	2	7	5	300	100	4	450	Dual, high speed

voltage regulators

DEVICE	V _O (V)	lo (mA)	IO (mA)	DROPOUT VOLTAGE (mV)	TOLERANCE (±%)	DESCRIPTION
2018 200	TYP	MAX	TYP	MAX		
TLV2217-33	3.3	500	2	500	1	Fixed 3.3 V, low dropout

p-channel MOSFETs

DEVICE	V _{DS} (V)	^r DS(on) (V _{GS} = -10 V) Ω	rDS(on) (V _{GS} = -4.5 V) Ω	rDS(on) (V _{GS} = -2.7 V) Ω	I _D (A)	DESCRIPTION				
	MAX	TYP	TYP	TYP	MAX					
TPS1100	-15	0.18	0.291	0.606	±1.58	Single p-channel enhancement-mode MOSFET				
TPS1101	- 15	0.09	0.134	0.232	±2.12	Single p-channel enhancement-mode MOSFET				



data acquisition and conversion

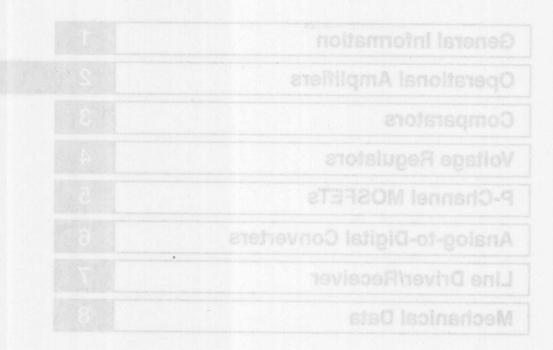
DEVICE	ADDRESS AND DATA I/O FORMAT	ANALOG SIGNAL INPUTS	RESOLUTION (BITS)	CONVERSION SPEED (µs)	TOTAL ERROR	DESCRIPTION			
TLV1543	Serial	11	10	21	±1 LSB	10-bit analog-to-digital converter			
TLV1549	Serial	i colona	10	21	±1 LSB	10-bit analog-to-digital converter			

TLV1549	Serial 1	0.55	21	±1L	SB	B 10-bit analog-to-digital con					
	mission circuits										
DEVICE	APPLICATION	BUS I/O		ERS/REC		8.0 8.0	260	DE	SCRIPT	ON	ANAGEVU EVERNU BEESVU
SN75LV4735	EIA Standard RS-232-D	Single ended	9	3/5	1.85	3.0	Multicha	nnel RS	5232 line	e driver/i	receiver

Single p-channel anharosment-mode MOSFET			



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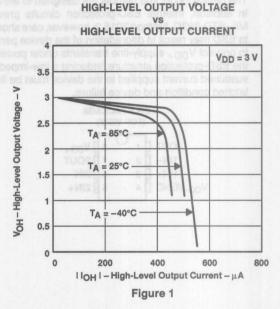
available features

- Output Swing Includes Both Supply Rails
- Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Low Power . . . 500 μA Max

description

The TLV2262 and TLV2262A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with upower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2262 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, VICR is specified with a larger maximum input offset voltage test limit of ± 5 mV,

- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage 950 μV Max at T_A = 25°C
- Wide Supply Voltage Range 2.7 V to 8 V
- Macromodel Included



allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 µA (typical) of supply current per amplifier, the TLV2262 family can achieve input offset voltage levels as low as 950 µV, outperforming existing CMOS amplifiers. The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

AVAILABLE OPTIONS

		PACKAGED DE	VICES		
TA	VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
-40°C to 85°C	950 μV 2.5 mV	TLV2262AID TLV2262ID	TLV2262AIP TLV2262IP	TLV2262AIPWLE	TLV2262Y

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLV2262IDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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PRODUCTION DATA information is current as of publication data. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.

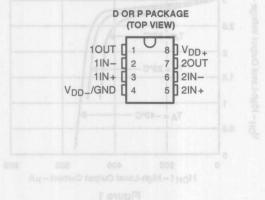


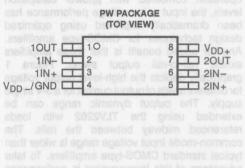
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description (continued)

The TLV2262 and TLV2262A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features combined with its temperature performance make the TLV2262 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.





adventage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is apecified with a larger mextmum inout offect voltage test limit of ± 5 mV.

allowing a minimum of 0 to 2-V common-mode input votage range for a 3-V supply. Furthermore, at 200 µA (typical) of supply current per adoplifier, the TL/2262 family can achieve input offset voltage levels as low as 850 µV, outperforming existing CMOS amplifiers. The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or expect levels offset devices descended or expective and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or expect levels offseted by top-gate JFET and expensive distective-isolated devices.

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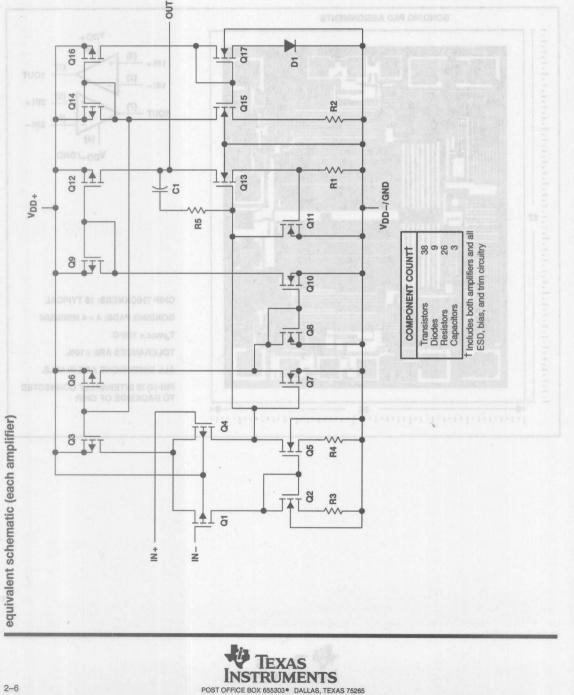
polycognosis amoralisation feeting on the

TLV2262Y chip information

BONDING PAD ASSIGNMENTS VDD+ and and a second and a second s (8) (3) 1IN+ (1) 10UT (2) 1IN-(5) 2IN+ 20UT (7) (6) 2IN-(4) VDD_/GND -67 F him and a second s **CHIP THICKNESS: 15 TYPICAL** BONDING PADS: 4 × 4 MINIMUM TJmax = 150°C TOLERANCES ARE ±10%. ALL DIMENSIONS ARE IN MILS. PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP. 56 իրություններութիրությունները

This chip, when properly assembled, displays characteristics similar to the TLV2262. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1) Differential input voltage, V _{ID} (see Note 2)	8 V
Input voltage range, V ₁ (any input, see Note 1) Input current, I ₁ (each input)	0.3 V to V _{DD}
Output current, Io	
Total current into V _{DD+}	
Total current out of V _{DD} Duration of short-circuit current (at or below) 25°C (see Note 3)	
Continuous total dissipation	
Operating free-air temperature range, TA	40°C to 85°C
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to VDD -.

- Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below VDD--0.3 V.
- The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
Р	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

				MIN	MAX	UNIT
Supply voltage, VDD± (see Note 1)	01	ephan Nort	VenVi	2.7	8	V
Input voltage range, VI	100	2550	ROM 1 - JR	V _{DD} -	V _{DD+} -1.3	V
Common-mode input voltage, VIC	stot	2510		V _{DD} -	V _{DD+} -1.3	V
Operating free-air temperature, TA			and the second	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to VDD -.

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8					1	TLV2262			LV2262/	Vion	8
	PARAMETER	TEST CON	DITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
aV of	V 8.0-			25°C	ON es	300	2500	Viegn	300	950	
VIO	Input offset voltage			Full range			3000	(each	d .mer	1500	μV
αΛΙΟ	Temperature coefficient of input offset voltage			25°C to 85°C		2		10 V 00	2	Aput cur tal cur	μV/°C
rimite stimite ideT p	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 1.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ $R_S = 50 \Omega$	25°C	olad 1	0.003	D	gV to 1 uonio-h uiseib li	0.003	tal oun nóiteu ouniteu	μV/m
10	Input offset current			25°C	e.Ta	0.5	NUISTOO	met ils	0.5	milated	рА
10	input onset current			Full range			150	atura	(empar	150	18 pr
IIB	Input bias current	minun		25°C	n) irom	001.01	(I) min	8,1 et	,teret,	net bei	рА
чв	input bias current	Austral of the Contractor	a transmission of the	Full range	Las results		150	-	ST. St	150	pr
na el "en	olition oo galatinaqo belariki	ntioder tebru bet slideles solves fo	net those indicates and the second states an	25°C	0 to 2	-0.3 to 2.2	i at these solutions	0 to 2	-0.3 to 2.2	ai opera Exposu	dindhon mpiled
VICR	Common-mode input voltage range	R _S = 50 Ω,	V _{IO} ≤5 mV	Full range	0 to 1.7	naihe a	ullo Agade Mil 16 ent I Dehorie	0 to 1.7	/ led name		V
		I _{OH} = -20 µA		25°C		2.99			2.99		
			BURST BHIT	25°C	2.85			2.85			
VOH	High-level output voltage	IOH = -100 μA		Full range	2.825	an Anna Anna Anna M		2.825			V
Voltage	voltage	I _{OH} = -200 µA	3-85 n AT 5700	25°C	2.7	104	2043	2.7			
		10H = -200 mA		Full range	2.65			2.65			
	V _{IC} = 1.5 V,	IOL = 50 μA	25°C	au non	10	c		10			
	Low-level output	V _{IC} = 1.5 V,	I _{OL} = 500 μA	25°C	The street	100			100		
VOL	voltage	VIC = 1.5 V,	ΙΟ <u>Γ</u> = 300 μΑ	Full range			150	······································		150	mV
		V _{IC} = 1.5 V,	I _{OL} = 1 mA	25°C		200			200		11008
				Full range		8 1 W 12 CA	300	0.312.00 140	do no	300	
	Large-signal differential	VIC = 1.5 V,	RL = 50 kه	25°C	60	100		60	100		
AVD	voltage amplification	$V_0 = 1 V \text{ to } 2 V$		Full range	30		()	30	100.00	l jegnilo	V/m\
V	1 400- Voor-12 1	Ŭ	$R_L = 1 M\Omega^{\ddagger}$	25°C		100			100	han beid	oy tug
^r id	Differential input resistance			25°C		1012		V, spa T	1012	i elborn-c	Ω
rj	Common-mode input resistance			25°C	14,0995	1012	mahlb k	9086.89	1012	Nov IIA	Ω
cj	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
zo	Closed-loop output impedance	f = 100 kHz,	Ay = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0 \text{ to } 1.7 \text{ V},$ $V_{O} = 1.5 \text{ V},$	R _S = 50 Ω	25°C Full range	65 60	75		65 60	77		dB
	Supply voltage	V _{DD} = 2.7 V to 8	RV.	25°C	80	95		80	100		
k SVR	rejection ratio (ΔV _{DD} /ΔV _{IO})	No load,	$V_{IC} = V_{DD}/2$	Full range	80		-	80		1	dB
IDD	Supply current	V _O = 1.5 V,	No load	25°C		400	500		400	500	
00	oupply our ent	VO = 1.5 V,	No load	Full range			500			500	μА

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

[†] Full range is – 40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



L	Leseet P	0.0001217				TLV2262		Т	LV2262A		
THU P	ARAMETER	TEST COND	ITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	080 000	0085 008	25°C	25°C	0.35	0.55		0.35	0.55		
SR	Slew rate at unity gain	$V_{O} = 1.1 V \text{ to } 1.9 V,$ $R_{L} = 50 k\Omega^{\ddagger},$	C _L = 100 pF‡	Full range	0.3			0.3	200 (51.042)	Terron	V/µs
V	Equivalent input	f = 10 Hz	0"38.pl	25°C	43			agash	43	of ingul	
Vn	noise voltage	f = 1 kHz	CORRE	25°C	Mo	V 8 12	day	ge long-	12	o hiqrif	nV/√H
	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C	SH	0.6		EN GIC	0.6	10 01105	
VN(PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz	Fell stoos	25°C		1		10	1	linput o	μV
In	Equivalent input noise current	1	28%	25°C		0.6			0.6	d tuqni	fA /√H:
-	Total harmonic	$V_{O} = 0.5 V \text{ to } 2.5 V,$	Av = 1	0.03%				0.03%			
THD + N distortion plus noise		f = 20 kHz, $R_L = 50 \text{ k}\Omega^{\ddagger}$	Av = 10	25°C		0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, $C_1 = 100 \text{ pF}^{\ddagger}$	$R_{L} = 50 \text{ k}\Omega^{\ddagger},$	25°C	121	0.67	UN I	3.00	0.67	Come voltage	MHz
BOM	Maximum output- swing bandwidth	$V_{O(PP)} = 1 V,$ $R_L = 50 k\Omega^{\ddagger},$	Ay = 1, CL = 100 pF‡	25°C		300	·Ho		300		kHz
Settling ti	Settling time	$A_V = -1$, Step = 1 V to 2 V,	To 0.1%	- 25°C	°C 12.5		- FIOI	5.6		ek rigitt	
	Setting time	$R_{L} = 50 \text{ k}\Omega^{\ddagger},$ $C_{L} = 100 \text{ pF}^{\ddagger}$	To 0.01%	25.0			12.5			μs	
φm	Phase margin at unity gain	R _L = 50 kه,	CL = 100 pF‡	25°C		61°	OV		61°		
	Gain margin	Den al al al	and an annual second second	25°C	In	14	Vinte		14		dB
	e is – 40°C to 85°C. ed to 1.5 V										
Reference											

ating characteristics at specified free-air temperature, V_{DD} = 3 V

T. Full range is ++ 40°C to 80°CL.

Relevanoed to 2,5 V

- regional values and bills at the input origin values with volume at through 200 froms of cristianal tit inst at TA = 100 from our



electrical characteristics at specified free-air temperature, V _{DD} = 5 V (unless	otherwise noted)
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Transfer 1	DADAMETED	TEST COL	IDITIONS	T. +	mount	LV2262		Т	LV2262	A	UNIT
	PARAMETER	TEST COM	IDITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Vie	Input offset voltage	0.65	28*C 0.36	25°C		300	2500		300	950	μV
VIO	input onset voitage			Full range		ECN.	3000	L. Un		1500	μν
ανιο	Temperature coefficient of input offset voltage	84		25°C to 85°C		2	H 01 = 1		2		μV/°C
	Input offset voltage long- term drift (see Note 4)	$V_{DD\pm} = \pm 2.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ R _S = 50 Ω	25°C		0.003	1 = 1 kH		0.003	noiso Pante	μV/m
*Va	1			25°C		0.5		100	0.5	vlupa	1000
10	Input offset current			Full range	25	01.07.2	150		voltage	150	рА
		8.0		25°C		1		100	1001	Equip	
IB	Input bias current			Full range			150		themus.	150	pA
Vice	Common-mode input	V _{IO} ≤5 mV	Rs = 50 Ω	25°C	0 to 4	-0.3 to 4.2	VO = 0V 1 - 20 k PL = 50	0 to 4	-0.3 to 4.2	isto otalo noise	t - CH
VICR	voltage range	0.67	NS = 50 22	Full range	0 to 3.5	2. 2 gE‡	1+ 1 kH 0[= 10	0 to 3.5		Gain- prédu	
219	1000	I _{OH} = -20 μA	0.62	25°C		4.99	08 = 19	ab	4.99	attiwa .	1.140
		I _{OH} = -100 μA		25°C	4.85	4.94	i-aut	4.85	4.94		
VOH	H High-level output voltage	10H = - 100 mA	man prach	Full range	4.82	Solv	Step « 1	4.82	posit or	det.o	V
		I _{OH} = -200 μA		25°C	4.7	4.85	08.9.18	4.7	4.85		
		10H = -200 mA		Full range	4.6			4.6			
	-18	V _{IC} = 2.5 V,	l _{OL} = 50 μA	25°C		0.01	10		0.01	aditta	
		V _{IC} = 2.5 V,	I _{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
VOL	Low-level output voltage	VIC = 2.0 V,	10L = 000 mA	Full range			0.15	012	8 of 010	0.15	V
		VIC = 2.5 V,	IOL = 1 mA	25°C		0.2	0.3		0.2	0.3	whole
		10 - 2.0 4,	IOL - THIN	Full range			0.3			0.3	
	Large-signal differential	V _{IC} = 2.5 V,	R _L = 50 kه	25°C	80	170		80	170		
AVD	voltage amplification	$V_{0} = 1 V \text{ to } 4 V$		Full range	55			55			V/m
		Ŭ	$R_L = 1 M\Omega^{\ddagger}$	25°C		550			550		
rid	Differential input resistance			25°C		1012			1012		Ω
rj	Common-mode input resistance			25°C		1012			1012		Ω
¢j	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
zo	Closed-loop output impedance	f = 100 kHz,	Av = 10	25°C		240			240		Ω
CMRR	Common-mode	VIC = 0 to 2.7 V,		25°C	70	83		70	83		dB
Simina	rejection ratio	$V_0 = 2.5 V_{,}$	R _S = 50 Ω	Full range	70			70			aB
kovp	Supply voltage rejection	V _{DD} = 4.4 V to 8		25°C	80	95		80	95		dB
ksvr	ratio (∆V _{DD} /∆V _{IO})	No load,	$V_{IC} = V_{DD}/2$	Full range	80			80			
DD	Supply current	V _O = 2.5 V,	No load	25°C		400	500		400	500	
00	ouppry current	V() = 2.5 V,	No load	Full range			500			500	μA

[†] Full range is – 40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^{\circ}$ C extrapolated to $T_A = 25^{\circ}$ C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



	DAMETER	TEOT CONDI	TIONO	- +		TLV2262		Т	LV2262/	A	UNIT
P	ARAMETER	TEST CONDI	TIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	
Val	0082 000		D Fallot	25°C	0.35	0.55		0.35	0.55	input o	0
SR	Slew rate at unity gain	$V_{O} = 1.5 V \text{ to } 3.5 V,$ $C_{L} = 100 \text{ pF}^{\ddagger}$	KL = 50 KΩ2+,	Full range	0.3			0.3	nuo laza emite esi	o lugni d lugni	V/µs
V	Equivalent input	f = 10 Hz		25°C		40			40		nV/√Hz
Vn	noise voltage	f = 1 kHz	30 m S 19	25°C	DIVI .	12	001 6080	W SADA	12	runer,	
	Peak-to-peak equivalent input	f = 0.1 Hz to 1 Hz		25°C	um	0.7			0.7		μV
V _N (PP)	noise voltage	f = 0.1 Hz to 10 Hz		25°C	HOI	1.3		CALEOV /A.	1.3		μν
In	Equivalent input noise current	Au 0 Au 00	10 = 10 10 = 10	25°C	OIV I	0.6		igistov ti	0.6	el-wa3	fA /√Hz
	Total harmonic	$V_{O} = 0.5 V \text{ to } 2.5 V,$ f = 20 kHz,	Ay = 1	25°C	OIV .	0.017%		(0.017%		
THD + N	distortion plus noise	$R_{L} = 50 \text{ k}\Omega^{\ddagger}$	Ay = 10	25 0	VOV	0.03%		latine si neite	0.03%	-otpâu trokov	dv/
9	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF‡	RL = 50 kه,	25°C		0.71	80	ntaken t	0.71	Dimeno	MHz
BOM	Maximum output- swing bandwidth	$V_{O(PP)} = 2 V,$ $R_{L} = 50 k\Omega^{\ddagger},$	Av = 1, CL = 100 pF‡	25°C	1 = 1	185	pao long	input ce	185	ຕາກເວລີ	kHz
Ba	Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V,	To 0.1%	25°C	DIV I	6.4	ollen f	olica(en	6.4	dimo0	μs
Eb	001 08	$R_{L} = 50 k\Omega^{\ddagger},$ $C_{L} = 100 pF^{\ddagger}$	To 0.01%	V 5.8 m	30V	14.1	ratio	nglection	14.1	Supply COVA)	RVR
φm	Phase margin at unity gain] R _L = 50 kΩ [‡] ,	CL = 100 pF‡	25°C	· <u>ov</u>	63°			63°	Supply	00
	Gain margin			25°C		14			14		dB

operating characteristics at specified free-air	temperature, $V_{DD} = 5 V$	
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[†] Full range is - 40°C to 85°C.

‡ Referenced to 2.5 V



-	DADAMETED	TEOT	CONDITIONS	TI	1	UNIT	
	PARAMETER	TEST	MIN	TYP	MAX		
VIO	Input offset voltage	120 0-25			300	2500	μV
10	Input offset current	$V_{DD} \pm = \pm 1.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ $R_S = 50 \Omega$	ST. On	0.5	150	pА
IIB	Input bias current	VO = 0,	ng = 00 22		1	150	pА
VICR	Common-mode input voltage range	V _{IO} ≤5 mV,	Rs = 50 Ω	0 to 2	-0.3 to 2.2	Gquiv ealon	V
	1 Park Israel and a star barre	ІОН = -20 μА	Sen i or sen rev	1	2.99	in the second	V
VOH	High-level output voltage	I _{OH} =200 μA	0,1 Hz (b 10 Hz	2.7	2.75	esion	V
		VIC = 0 V,	lol = 50 μA	1 10	10	Equiv	
VOL	Low-level output voltage	V _{IC} = 0 V,	l _{OL} = 500 μA		100	125	V
	0.017% 0.017%	V _{IC} = 0 V,	I _{OL} = 1 mA	1	200	250	
A	Large-signal differential	$V_{O} = 1 V \text{ to } 2 V$	$R_L = 50 k\Omega^{\dagger}$	60	100	distort	V/m
AVD	voltage amplification	VO = 1 V to 2 V	$R_L = 1 M\Omega^{\dagger}$		100		v/m
rid	Differential input resistance	2785 25°C	oo ana oo taxaa ah	11 10	1012	PERSENT.	Ω
rj	Common-mode input resistance				1012		Ω
Cj	Common-mode input capacitance	f = 10 kHz	training training		8	inemin Selves	pF
z _o	Closed-loop output impedance	f = 100 kHz,	Ay = 10		270	-	Ω
CMRR	Common-mode rejection ratio	VIC = 0 to 1.7 V,	$V_{O} = 0$, $R_{S} = 50 \Omega$	65	77		dB
ksvr	Supply voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	$V_{DD} = 2.7 V \text{ to } 8 V,$	No load, $V_{IC} = 0$	80	100		dB
IDD	Supply current	V _O = 0,	No load	10	400	500	μA

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)



			00110110110	TLV2262Y			UNIT
	PARAMETER	TEST	TEST CONDITIONS			MAX	
VIO	Input offset voltage				300	2500	μV
10	Input offset current	$V_{DD\pm} = \pm 2.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ Rs = 50 Ω		0.5	150	pА
IB	Input bias current	v() = 0,	115 - 00 22	ALC: N	1	150	pА
VICR	Common-mode input voltage range	V _{IO} ≤5 mV,	R _S = 50 Ω	0 to 4	-0.3 to 4.2		V
		I _{OH} = -20 μA	spanos.	tugel	4.99	VIII	
VOH	High-level output voltage	I _{OH} = -100 μA	and the second property of	4.85	4.94	-	V
		IOH = -200 µА	and the second se	4.7	4.85		
	at for set when to the form	V _{IC} = 2.5 V,	loL = 50 μA		0.01	2	
VOL	Low-level output voltage	V _{IC} = 2.5 V,	ΙΟΕ = 500 μΑ		0.09	0.15	V
	kt uit Preventionen houpen	V _{IC} = 2.5 V,	I _{OL} = 1 mA	hori8	0.2	0.3	
A	Large-signal differential	VIC = 2.5 V,	$R_L = 50 k\Omega^{\dagger}$	80	170		V/m\
AVD	voltage amplification	$V_0 = 1 V \text{ to } 4 V$	$R_L = 1 M\Omega^{\dagger}$	in the second	550	-	v/mv
rid	Differential input resistance		and the second		1012		Ω
rj	Common-mode input resistance				1012		Ω
ci	Common-mode input capacitance	f = 10 kHz	and the second		8	-	pF
zo	Closed-loop output impedance	f = 100 kHz,	Ay = 10	12.4.5	240		Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V,	$V_{O} = 2.5 V$, $R_{S} = 50 \Omega$	70	83	0	dB
SVR	Supply voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	V _{DD} = 4.4 V to 8 V,	No load, $V_{IC} = V_{DD}/2$	80	95		dB
IDD	Supply current	V _O = 2.5 V,	No load	-	400	500	μΑ

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

† Referenced to 2.5 V

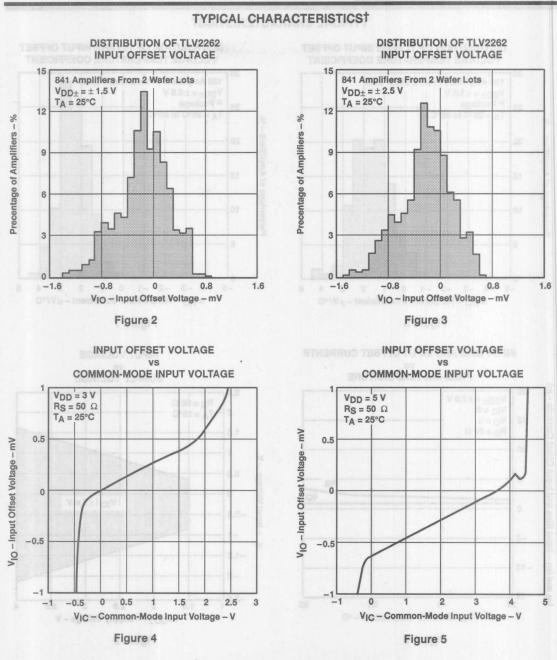
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The second mean second se	



	-	Table of Graphs				
	2.0	Dage No.	Distribution	FIGURE		
	VIO	Input offset voltage		2,3		
		Input offset voltage temperature coefficient	vs Common-mode voltage Distribution			
	avio			6, 7 8		
	IIB/IIO	Input bias and input offset currents	vs Free-air temperature			
	VI REA	Input voltage	vs Supply voltage	9		
	Maria	Lieb level extend veloce	vs Free-air temperature	10		
	VOH	High-level output voltage	vs High-level output current	11, 14		
	VOL	Low-level output voltage	vs Low-level output current	12, 13, 15		
	VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	16		
	los	Short-circuit output current	vs Supply voltage	17		
			vs Free-air temperature	18		
	VID	Differential input voltage	vs Output voltage	19, 20		
	Stor		vs Load resistance	21		
AVD	AVD	Differential voltage amplification	vs Frequency	22, 23		
			vs Free-air temperature	24, 25		
	ZO	Output impedance	vs Frequency	26, 27		
	CMRR	Common-mode rejection ratio	vs Frequency	28		
		and a second	vs Free-air temperature	29		
	KSVR	Supply-voltage rejection ratio	- Contraction	30, 31		
	-	2	vs Free-air temperature	32		
	IDD	Supply current	vs Free-air temperature	33		
	SR	Slew rate	vs Load capacitance	34		
			vs Free-air temperature	35		
	Vo	Large-signal pulse response	vs Time	36, 37, 38, 39		
	Vo	Small-signal pulse response	vs Time	40, 41, 42, 43,		
	Vn	Equivalent input noise voltage	vs Frequency	44, 45		
		Noise voltage (referred to input)	Over a 10-second period	46		
		Integrated noise voltage	vs Frequency	47		
	THD + N	Total harmonic distortion plus noise	vs Frequency	48		
		Gain-bandwidth product	vs Free-air temperature	49		
			vs Supply voltage	50		
	φ _m	Phase margin	vs Frequency	22, 23		
			vs Load capacitance	51		
		Gain margin	vs Load capacitance	52		
	B ₁	Unity-gain bandwidth	vs Load capacitance	53		
		Overestimation of phase margin	vs Load capacitance	54		

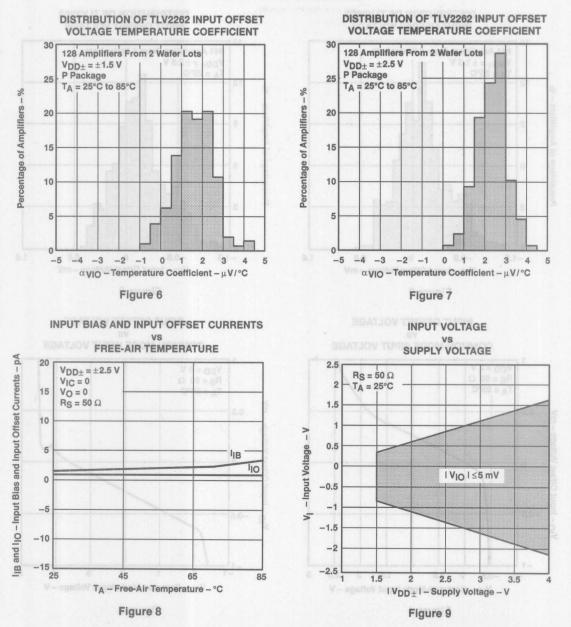
TYPICAL CHARACTERISTICS





⁺ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

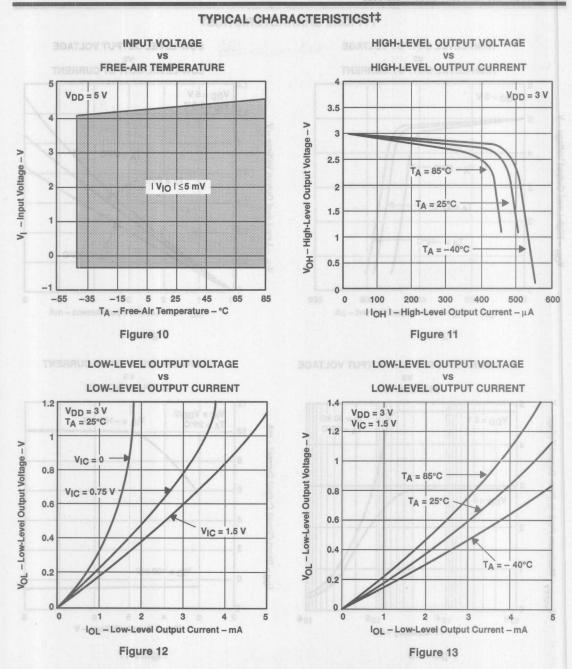




TYPICAL CHARACTERISTICS[†]

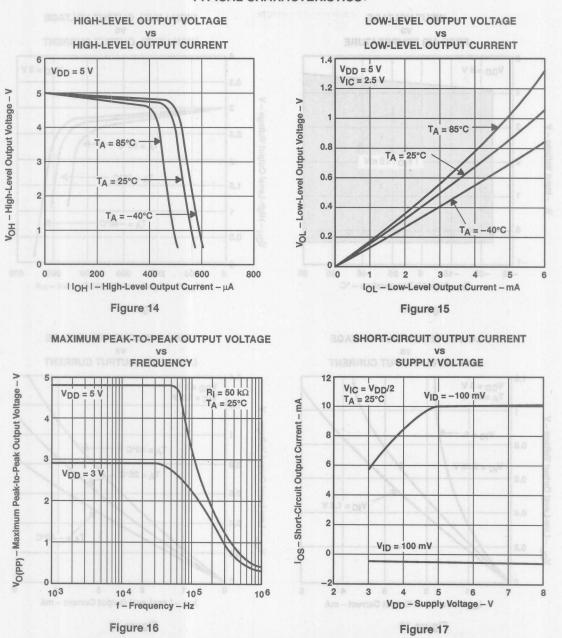
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

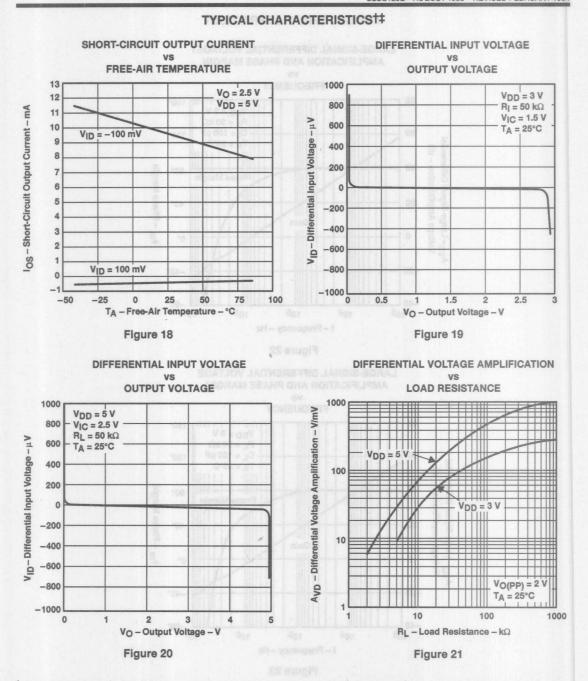




TYPICAL CHARACTERISTICS[†]

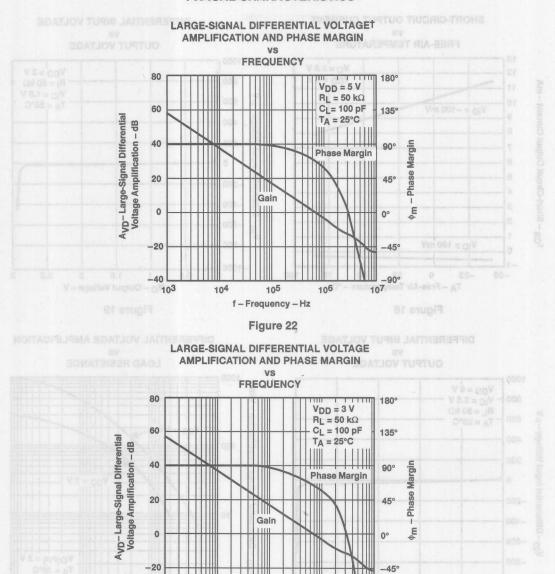
⁺ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.





[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.





-90°

107

106

TYPICAL CHARACTERISTICS[†]

-40

103

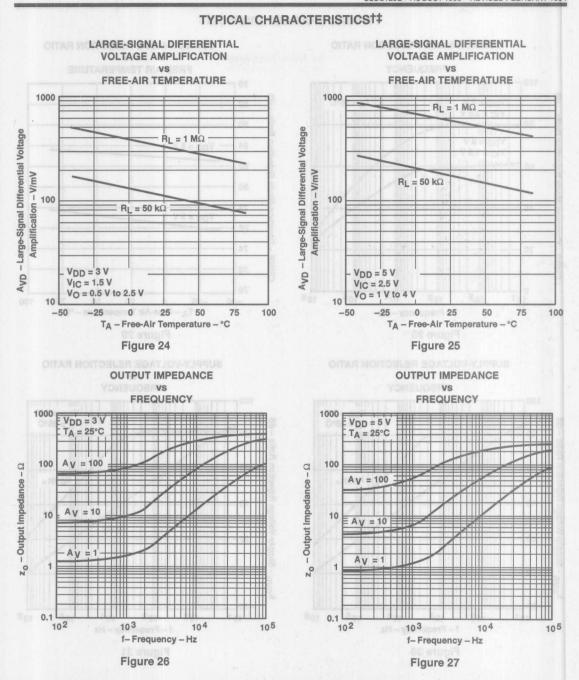
104

10⁵ f – Frequency – Hz Figure 23

⁺ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

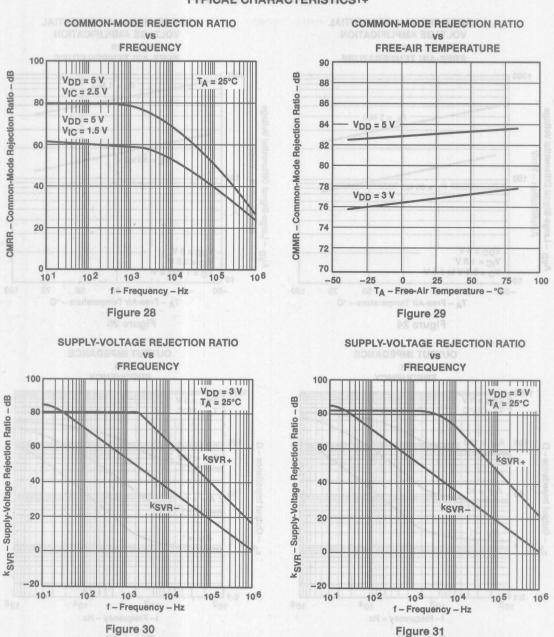
IEXAS INSTRUMENTS

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[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.





TYPICAL CHARACTERISTICS^{†‡}

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS^{†‡} SUPPLY-VOLTAGE REJECTION RATIO SUPPLY CURRENT VS VS **FREE-AIR TEMPERATURE FREE-AIR TEMPERATURE** 110 600 VDD = 2.7 V to 8 V k_{SVR} - Supply-Voltage Rejection Ratio - dB $V_{IC} = V_O = V_{DD}/2$ 500 105 - Supply Current - µA VDD = 5 V Vo = 2.5 V 100 400 VDD = 3 V Vo = 1.5 V DD 95 300 90 200 -50 -25 0 25 50 75 100 -50 -25 0 25 50 75 TA - Free-Air Temperature - °C TA - Free-Air Temperature - °C Figure 32 Figure 33 **SLEW RATE** SLEW RATE VS VS LOAD CAPACITANCE FREE-AIR TEMPERATURE 1.2 SR-1 0.8 SR SR - Slew Rate - V/µ s SR - Slew Rate - V/µ s 0.8 SR+ 0.6 0.6 SR+ 0.4 0.4 $V_{DD} = 5 V$ 0.2

0.2 $V_{DD} = 5 V$ $R_L = 50 k\Omega$ CL = 100 pF $A_V = -1$ TA = 25°C Ay = 10 102 103 104 -50 -25 0 25 50 CL - Load Capacitance - pF TA - Free-Air Temperature - °C Figure 34 Figure 35

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

0

101

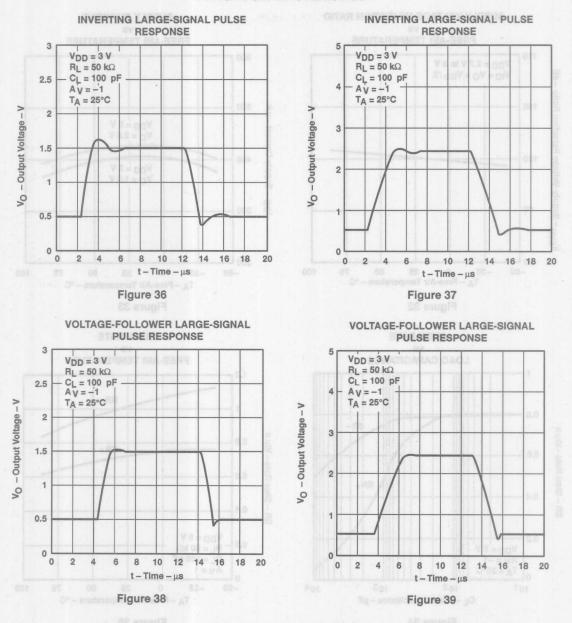


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75

100

TLV2262, TLV2262A, TLV2262Y Advanced LinCMOSTM RAIL-TO-RAIL DUAL OPERATIONAL AMPLIFIERS SLOS129B – AUGUST 1993 – REVISED FEBRUARY 1994



TYPICAL CHARACTERISTICS^{†‡}

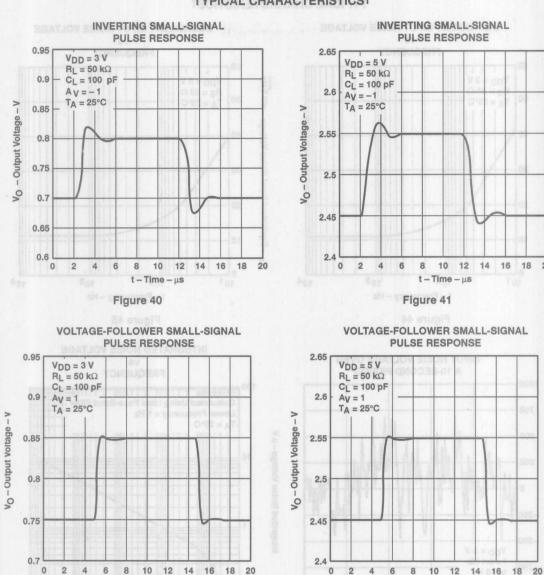
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.



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t-Time-µs

Figure 43



TYPICAL CHARACTERISTICS[†]

[†] For all curves where VDD = 5 V, all loads are referenced to 2.5 V. For all curves where VDD = 3 V, all loads are referenced to 1.5 V.

t-Time-µs

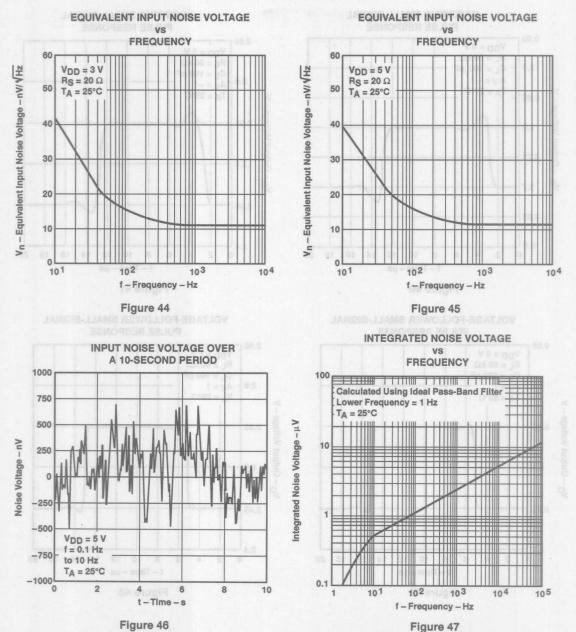
Figure 42



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TLV2262, TLV2262A, TLV2262Y Advanced LinCMOSTM RAIL-TO-RAIL DUAL OPERATIONAL AMPLIFIERS SLOS129B – AUGUST 1993 – REVISED FEBRUARY 1994



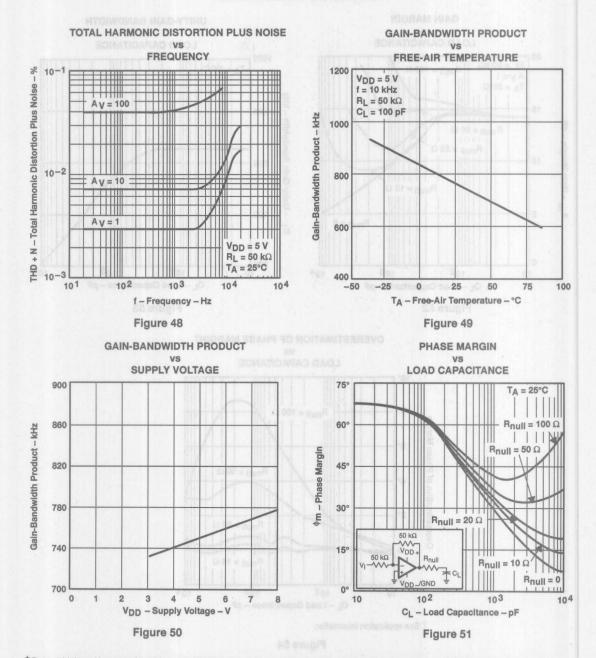


⁺ For all curves where VDD = 5 V, all loads are referenced to 2.5 V. For all curves where VDD = 3 V, all loads are referenced to 1.5 V.



TLV2262, TLV2262A, TLV2262Y Advanced LinCMOS™ RAIL-TO-RAIL DUAL OPERATIONAL AMPLIFIERS SLOS129B – AUGUST 1993 – REVISED FEBRUARY 1994

TYPICAL CHARACTERISTICS^{†‡}

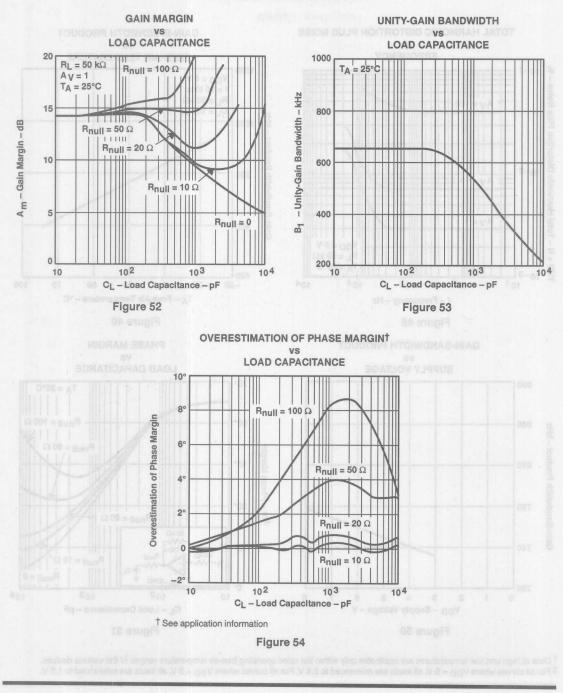


[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.



TLV2262, TLV2262A, TLV2262Y Advanced LinCMOSTM RAIL-TO-RAIL DUAL OPERATIONAL AMPLIFIERS SLOS129B – AUGUST 1993 – REVISED FEBRUARY 1994







APPLICATION INFORMATION

loading considerations

The TLV2262 is a low-voltage, low-power version of the TLC2272 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2262 is similar to the TLC2272 and is capable of driving several milliamperes.

The design topology used for the TLV2262 or the TLV2272 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. While the TLV2272 is capable of greater than 1-mA drive from the positive rail, the TLV2262 is capable of only a few hundred microamperes. When designing with lower impedance loads (less than 50 k Ω) with the TLV2262, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2262 topology provides lower drive to the positive rail than other high-output-drive rail-to-rail operational amplifiers, it is a more stable topology.

driving large capacitive loads

The TLV2262 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω , 20 Ω , 50 Ω , and 100 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta \theta_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times \text{R}_{\text{null}} \times \text{C}_{\text{I}} \right)$$

where : $\Delta \theta_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

 $C_1 = load capacitance$

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$F = \frac{1}{1 + g_m \times R_{null}}$$

(2)

(1)

where : F = factor reducing frequency of pole

 $g_m = \text{small-signal output transconductance (typically 4.83 × 10⁻³ mhos)}$

R_{null} = output series resistance



TLV2262, TLV2262A, TLV2262Y Advanced LinCMOSTM RAIL-TO-RAIL DUAL OPERATIONAL AMPLIFIERS SLOS129B - AUGUST 1993 - REVISED FEBRUARY 1994

APPLICATION INFORMATION

driving large capacitive loads (continued)

For the TLV2262, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L : at $C_L = 10$ pF, use 60 MHz, at $C_L = 1000$ pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation (1) to better approximate the improvement in phase margin.

$$\Delta \theta_{m2} = \tan^{-1} \left[\frac{UGBW}{(F \times P_2)} \right] - \tan^{-1} \left(\frac{UGBW}{P_2} \right)$$

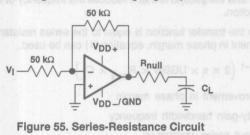
where : $\Delta \theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation (2)

P₂ = unadjusted pole (60 MHz @ 10 pF, 6 MHz @ 100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.



The unity-gain bandwidth (UGBW) trequency decreases as the capacitive load increases (see Figure 33). To use equation (1), UGBW must be approximated from Figure 33.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The everestimation is caused by the decrease in the frequency of the pole associated with the load, providing idditional phase shift and reducing the overall improvement in phase margin. The pole associated with the load a reduced by the factor calculated in equation (2).

(3)

where t IF = factor reducing frequency of pole

on = small-signal output transconductance (typically 4.83 x 10⁻¹² mhos)

Rena = output series resistance



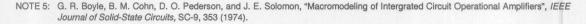
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using $PSpice^{\textcircled{B}}$ PartsTM model generation software. The Boyle macromodel and subcircuit in Figure 56 are generated using the TLV2262 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit



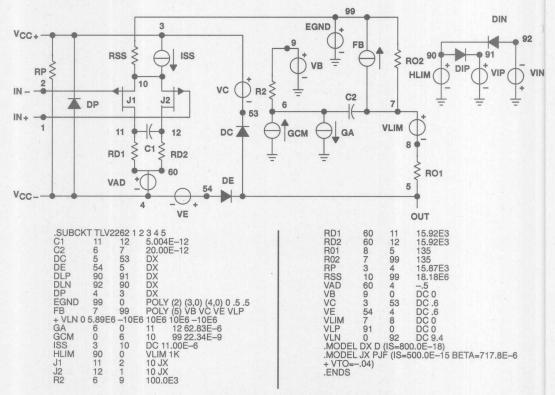


Figure 56. Boyle Macromodel and Subcircuit

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TLV2262, TLV2262A, TLV2262Y Advanced LincMQS** RAIL-TO-RAIL DUAL OPERATIONAL AMPLITERS

APPLICATION INFORMATION

mecromodel information

Desire Collins and the

Iscromodel Information provided is derived using PSpice® Parts[™] model generation software. The Boyle nacromodel and subcircuit in Figure 56 are generated using the TLV2262 typical electrical and operating hareoteristics at T_A = 26°C. Using this information, output simulations of the following key parameters can be entrated to a tolerance of 20% (in most cases).

- Maximum positive output voltage swing
- Maximum negative output vollage swing
 - Slaw rate
 - Ouisscent power dia
 - Inertal rise correct
 - Open-loop voltage ambilification

- Voleupent nise-vintu = #
- Common-mode rejection ratio
 - nicasm eserta
 - OC output resistance
 - AC output resistance
- Final Inerrus Justice Surrent limit



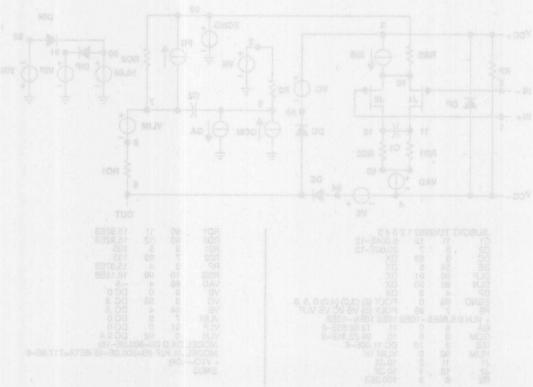


Figure 38. Boyle Macromodel and Suboledult

Soba is a registered tredemark of Microbim Corporator.

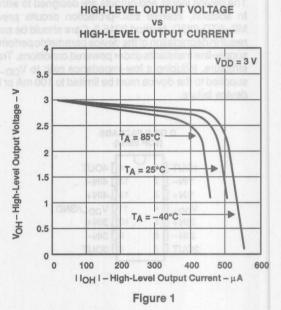
available features

- Output Swing Includes Both Supply Rails
- Low Noise . . . 12 nV/ \sqrt{Hz} Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Low Power . . . 1 mA Max

description

The TLV2264 and TLV2264A are guad operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with upower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOStype amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2264 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, VICB is specified with a larger maximum input offset voltage test limit of

- Common-Mode Input Voltage Range
 Includes Negative Rail
- Low Input Offset Voltage 950 μV Max at T_A = 25°C
- Wide Supply Voltage Range
 2.7 V to 8 V
- Macromodel Included



 \pm 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 µA (typical) of supply current per amplifier, the TLV2264 family can achieve input offset voltage levels as low as 950 µV outperforming existing CMOS amplifiers. The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

AVAILABLE OPTIONS

A DESCRIPTION OF		PACKAGED DEVICES					
TA	VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	CHIP FORM (Y)		
-40°C to 85°C	950 μV 2.5 mV	TLV2264AID TLV2264ID	TLV2264AIN TLV2264IN	TLV2264AIPWLE	TLV2264Y		

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLV2264IDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

Advanced LinCMOS™ is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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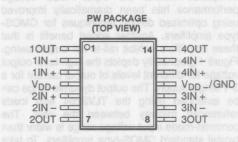
2-33

description (continued)

The TLV2264 and TLV2264A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power-dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to analog-to-digital converters (ADCs). All of these features, combined with its temperature performance make the TLV2264 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-} /GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

DO		VIEW)	GE
10UT [1	14] 40UT
1IN-[2	13] 4IN-
1IN+[3	12] 4IN+
VDD+[4	11	VDD_/GND
2IN+[5	10] 3IN+
2IN-[6	9	3IN-
20UT	7	8	3OUT



advantage of this improvement in performence and to make this device available for a wider range of applications, V_{ECR} is specified with a terge

a) 5 mM, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 µA. (typical) of supply current per amplitier, the TUV2284 family can achieve input offset voltage levels as iow as 950 µV outperforming existing CMOS amplifiers. This Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time lina time access to a solic or exceed technology to obtain input offset voltage stability with temperature and time lina time access to a solicanable using metal-gate technology. This technology also makes possible input-impedance levels that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive disectric-isolated devices.

he D packages are available toped and realed. And R authy to device type, (e.g., TLV2264IDR).

no PW peologento available only lath-end tapad and realed. Chips are tested at 25%,



TLV2264Y chip information

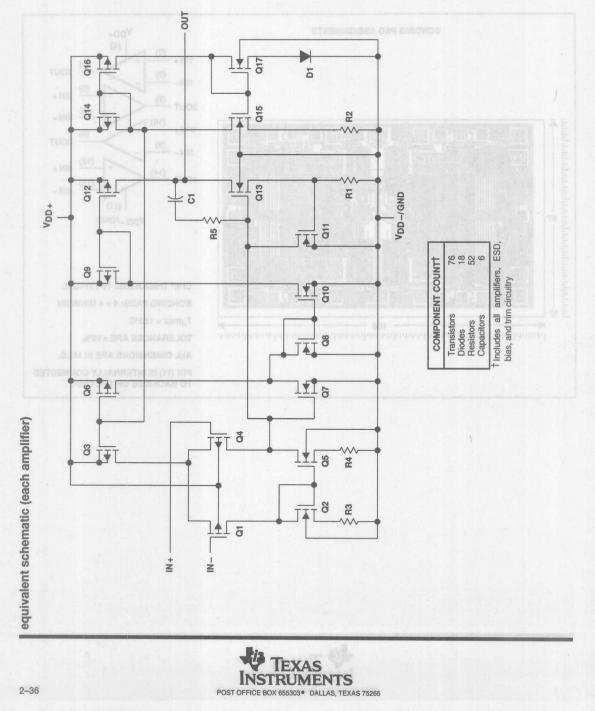
BONDING PAD ASSIGNMENTS VDD+ (4) (3) 1IN+ (1) 10UT (2) 1IN-(5) 2IN+ 20UT (7) (6) 2IN-3IN+ (10) (8) 3IN - (9) **3OUT** (14 (12) 4IN+ 40UT (14) (13) 4IN-(11) 67 VDD_/GND (1) (7 **CHIP THICKNESS: 15 TYPICAL** (3 **BONDING PADS: 4 × 4 MINIMUM** TJmax = 150°C 109 նաստեստանանանանին անկանություններու անդանանին անկանություն TOLERANCES ARE ±10%. ALL DIMENSIONS ARE IN MILS. PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

This chip, when properly assembled, displays characteristics similar to the TLV2264. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.



CLV2284V chib Information

This duip, whan property assembled, displays characteristics similar to the TLV2264. Thermal compression or ultrasonic bonding may be used on the doped atuminum bonding pads. The onip may be mounted with conductive epoxy or a gold-silicon preform.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1) Differential input voltage, V _{ID} (see Note 2)	
Input voltage range, V ₁ (any input, see Note 1) Input current, I ₁ (each input)	
Output current, Io	±50 mA
Total current into V _{DD+}	
Total current out of V _{DD} _	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, TA	–40°C to 85°C
Storage temperature range	
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to VDD -.

- Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below VDD – 0.3 V.
- The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

	DISSIPATIO	ON RATING TABLE	
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE $T_A = 25^{\circ}C$	T _A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

	60 100	100	60	0/85	town of		MIN	MAX	UNIT
Supply vo	Itage, $V_{DD\pm}$ (see Note	1)	30	Fullrange	and and	Vol Vincy	2.7	8	V
Input volta	age range, V _I	007		28*0	_ FL = 1 MΩF		V _{DD} -	V _{DD+} -1.3	V
Common-	mode input voltage, VIC	1012		2996			VDD-	V _{DD+} -1.3	V
Operating	free-air temperature, T	A			and the second		-40	85	°C
NOTE 1: /	All voltage values, exce	pt differential vo	ltages, a	are with respec	ct to V _{DD}		9	anatelem kuqni	n
						V(Q = 0 to 1.7) Rg = 80 D			
								Supply voltage	
	08								

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8					1	FLV2264	MA and	Т	LV2264/	A	0
	PARAMETER	TEST CON	IDITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
noVo	V. E. Owner			25°C	tol/i as	300	2500	Vision	300	950	
VIO	Input offset voltage			Full range			3000	ricest	d iner	1500	μV
ανιο	Temperature coefficient of input offset voltage			25°C to 85°C		2		o Von	2	ntput o	μV/°(
e60 m atimite tdeïl e	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 1.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ $R_S = 50 \Omega$	25°C	oled w	0.003	0- Shuo II setion	tol V _C voio ti lealti	0.003	nuo tes notien: oueitro	μV/m
lio	Input offset current			25°C	AT O	0.5	utetec	met siz	0.5	otratio	pA
10	input onset current	· · · · · · · · · · · · · · · · · · ·		Full range	and see	and the second	150	alure r	nacimal	150	2 pr
260%	Input bias current			25°C	nont (d	oni (1)	1) mm	8.1.91	the left	nel ber	pA
IB	input bias current	and a factor of the second		Full range	and miles	Lauren dette	150		a and	150	PA
on ai "an	nanded operating condition	moori" tebru bel	soloni asorti bre	25°C	0 to	-0.3 to	esch le i	0 to	-0.3 to	shirijā la	undrian
	Common-mode input	andesen solved to		25 0	2	2.2	emumes Recenses	2	2.2		100000
VICR	voltage range	R _S = 50 Ω,	V _{IO} ≤5 mV	I with respi	0	No bone	10 30	0	/ lplineno	2, 131	V
				Full range	to			to			
umixan	nied to ensure that the	ollages must be	s Andelma zo, puta	outpeopresi	1.7	torilite as	tretterte	1.7	Juquo I	S. 1978	
		I _{OH} = -20 μA		25°C		2.99		di Cines	2.99		
	High-level output	ІОН = -100 μА	BJBAT DHIT	25°C	2.85			2.85			
VOH	voltage	10H = - 100 mA	aroaa ostaras	Full range	2.825			2.825			V
	EMIT	I _{OH} = -200 µA		25°C	2.7	109	367678	2.7			
		im LPL	OPMm B X	Full range	2.65		13	2.65			-
		$V_{IC} = 1.5 V,$	IOL = 50 μA	25°C		10			10		
V.e.	Low-level output	VIC = 1.5 V,	IOL = 500 μA	25°C		100	150		100	150	
VOL	voltage			Full range 25°C		200	150		200	150	mV
		V _{IC} = 1.5 V,	IOL = 1 mA	Full range		200	300	101010	200	300	noo
THE	T YAM DOM T			25°C	60	100	300	60	100	300	
AVD	Large-signal differential	V _{IC} = 1.5 V,	$R_L = 50 k\Omega^{\ddagger}$	Full range	30	100	12	30	100	t and the	V/m
AVD	voltage amplification	$V_{O} = 1 V \text{ to } 2 V$	$R_I = 1 M\Omega^{\ddagger}$	25°C		100		00	100		V/III
- V	Differential input							and and a			201 200
rid	resistance	and the second s		25°C		1012		T and the	1012		Ω
rj	Common-mode input resistance		rio V ₀₀	25°C	nges, in	1012	aysillb Ic	80769 ,81	1012	llov IA	Ω
ci	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
zo	Closed-loop output impedance	f = 100 kHz,	A _V = 10	25°C		270			270		Ω
CMRR	Common-mode	V _{IC} = 0 to 1.7 V,	V _O = 1.5 V,	25°C	65	75		65	77		dB
	rejection ratio	R _S = 50 Ω		Full range	60			60			uD
ksvr	Supply voltage rejection ratio	$V_{DD} = 2.7 V \text{ to } $ No load,	3 V, VIC = VDD/2	25°C	80	95		80	100		dB
in de	$(\Delta V_{DD}/\Delta V_{IO})$,	10 = 100,2	Full range	80			80			
DD	Supply current	Vo = 1.5 V,	No load	25°C		0.8	1		0.8	1	mA
	(four amplifiers) nge is - 40°C to 85°C.			Full range			1			1	

electrical characteristics at specified free-air temperature Van - 3 V (unless otherwise noted)

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at TA = 150°C extrapolated to $T_A = 25^{\circ}C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



THE .	ALIGNESVOT				artare arta	TLV2264		Т	LV2264A	in man	
PA	RAMETER	TEST CONE	DITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
SR	Slew rate at unity	$V_{O} = 0.7 \text{ V to } 1.7 \text{ V},$	R _L = 50 kΩ [‡] ,	25°C	0.35	0.55		0.35	0.55	ho luqui	Ning
SR	gain	C _L = 100 pF‡	26°C	Full range	0.3			0.3		heighteit Aussian	V/µs
Vn	Equivalent input	f = 10 Hz		25°C		43			43		nV/√H:
*n	noise voltage	f = 1 kHz	Crisc ,	25°C	MON	12	\$004		12	iono-len	1197911
	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		N
V _N (PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz	Apple Ru?	25°C		1			en.o. 1 e	no sugra	μV
In	Equivalent input noise current	lan la	25%0	25°C		0.6			0.6	id han	fA /√H:
THD + N	Total harmonic distortion plus	$V_{O} = 0.5 V \text{ to } 2.5 V,$ f = 20 kHz,	Ay = 1	25°C		0.03%			0.03%		
	noise	$R_{\rm L} = 50 \ \rm k\Omega^{\ddagger}$	Ay = 10	250		0.05%		haten	0.05%	-	
	Gain-bandwidth product	f = 1 kHz, C _L = 100 pF‡	R _L = 50 kه,	25°C		0.67	1094		0.67		MHz
BOM	Maximum output- swing bandwidth	VO(PP) = 1 V, R _L = 50 kه,	A _V = 1, C _L = 100 pF‡	25°C		300	- Hol		300		kHz
ts	Settling time	$A_V = -1$, Step = 1 V to 2 V,	To 0.1%	25°C	1	5.6	- HOI		5.6	al-rigit-	110
'S	Setting time	$R_{L} = 50 \text{ k}\Omega^{\ddagger},$ $C_{L} = 100 \text{ pF}^{\ddagger}$	To 0.01%	200		12.5	=HOI		12.5		μs
φm	Phase margin at unity gain	R _I = 50 kه,	C _L = 100 pF‡	25°C	- 301	61°	- 0M		61°		
V	Gain margin		0[= 100 pr 1	25°C	100	14	10.00		14	VOLVOL	dB
	e is – 40°C to 85°C. ed to 1.5 V	0.0 5.0	28.0	Amil	- 101	Vas	Vio =1				
- Heterenc											
						Vas					



	PARAMETER	TEST CON	DITIONS	- +	۲	LV2264		Т	LV2264/	1	LINUT
	PARAMETER	TEST CON	DITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Vie	Innut offert veltere	88.0	28-0 0.35	25°C	1	300	2500		300	950	μV
VIO	Input offset voltage			Full range	肩ール	3.7 G V	3000	v viin	u te ofer	1500	μν
αΛΙΟ	Temperature coefficient of input offset voltage			25°C to 85°C		2	001 = 1		2	gain	μV/°C
HANN	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ $R_S = 50 \Omega$	25°C		0.003	11412 101110		0.003	eden oolaa Pesk	μV/mo
Va	Input offset current			25°C		0.5		11	0.5	A JOSPIE	pA
10	input onset current			Full range		aron or	150	1	affinition.	150	PA
IIB	Input bias current	8.0		25°C		1		10	on in tis	viup3	рА
чв	input bias ourroint			Full range		-	150	1	ND651UD	150	PA
	Common-mode input	0.03%	0485	25°C	0 to 4	-0.3 to 4.2	0 = 0.3 - 20 M L = 50 M	0 to 4	-0.3 to 4.2		* - OH V
VICR	voltage range	V _{IO} ≤5 mV,	Rs = 50 Ω	Full range	0 to 3.5	\$ 30	sHk 1- 007 = 3	0 to 3.5	bent/wid Io	Gain- produ	
10	005	I _{OH} = -20 μA	12/62	25°C	0	4.99	102.77	a la cas	4.99	and and a	MO
				25°C	4.85	4.94		4.85	4.94		
VOH	High-level output voltage	IOH = -100 μA		Full range	4.82	N C AF	11-000	4.82	in the second		V
	voltage	I _{OH} = -200 µA		25°C	4.7	4.85	£ = 150 kg	4.7	4.85	and the second	1
	0,51	10H = -200 MA	14 PT	Full range	4.6	1.90	001 - 1	4.6			
		V _{IC} = 2.5 V,	loL = 50 μA	25°C		0.01		1 18	0.01	Phone	
	Low-level output	$V_{IC} = 2.5 V_{,}$	IOL = 500 μA	25°C	19.	0.09	0.15	1	0.09	0.15	-11
VOL	voltage	10 - 2.0 1,	10L - 000 mr	Full range			0.15		dignam	0.15	V
		VIC = 2.5 V,	$I_{OL} = 1 \text{ mA}$	25°C		0.2	0.3	.0°8	0.2	0.3	ruen dui
		10	OL	Full range			0.3		V 6.	0.3	The Tephizi
	Large-signal differential	$V_{IC} = 2.5 V_{,}$	RL = 50 kه	25°C	80	170		80	170		
AVD	voltage amplification	$V_0 = 1 V \text{ to } 4 V$		Full range	55			55			V/m\
-	Differential innut		R _L = 1 MΩ [‡]	25°C		550			550		-
rid	Differential input resistance			25°C		1012			1012		Ω
rj	Common-mode input resistance			25°C		1012			1012		Ω
ci	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
zo	Closed-loop output impedance	f = 100 kHz,	Ay = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, Rs = 50 Ω	V _O = 2.5 V,	25°C Full range	70 70	83		70 70	83		dB
koup	Supply voltage rejection ratio	V _{DD} = 4.4 V to 8	V,	25°C	80	95		80	95		15
ksvr	$(\Delta V_{DD}/\Delta V_{IO})$	No load,	$V_{IC} = V_{DD}/2$	Full range	80			80			dB
DD	Supply current	$V_{O} = 2.5 V_{,}$	No load	25°C		0.8	1		0.8	1	mA

† Full range is – 40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^{\circ}$ C extrapolated to $T_A = 25^{\circ}$ C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



	TLV22SAY					TLV2264		Т	LV22644	4	
PA	RAMETER	TEST COND	ITIONS	TAT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
. Vii	Slew rate at unity	$V_{O} = 1.4 \text{ V to } 2.6 \text{ V},$	$R_{I} = 50 k\Omega^{\ddagger}$	25°C	0.35	0.55		0.35	0.55	eluqui,	01
SR	gain	$C_L = 100 \text{ pF}^{\ddagger}$	nL = 50 K22+,	Full range	0.3			0.3	nuo tech mun col	npot o 10qn	V/µs
V	Equivalent input	f = 10 Hz		25°C		40			40		nV/√Hz
Vn	noise voltage	f = 1 kHz	Ud w BH	25°C	OIV I	12	in geral	NY EDGAL	12	Mindau	
V	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C	- 14051	0.7			0.7		
VN(PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C	- HOL	1.3			1.3		μV
In v	Equivalent input noise current	Au o	101 × 101	25°C	* 01V	0.6		n voltage	0.6	Low-in	fA /√Hz
THE N	Total harmonic	$V_{O} = 0.5 V \text{ to } 2.5 V,$	Ay = 1	0500	- 01V	0.017%			0.017%		
THD + N	distortion plus noise	f = 20 kHz, $R_L = 50 \text{ k}\Omega^{\ddagger}$	Ay = 10	- 25°C	= .0V	0.03%		forential stice	0.03%	-ogiil.}	ave
0	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF‡	R _L = 50 kه,	25°C		0.71	ear	utsizer, f	0.71	Dittore	MHz
BOM	Maximum output- swing bandwidth	$V_{O(PP)} = 2 V,$ $R_{L} = 50 k\Omega^{\ddagger},$	Av = 1, CL = 100 pF‡	25°C	07 = 10	185	neinan	na tueni)	185	mmnä	kHz
86	Settling time	$A_V = -1$, Step = 0.5 V to 2.5 V,	To 0.1%	25°C	- 01V	6.4	1.1%10	ngaalau	6.4	mma0	
ts Bb	001 08	$R_{L} = 50 k\Omega^{\ddagger},$ $C_{L} = 100 pF^{\ddagger}$	To 0.01%	250	dov	14.1	olisi	nejectica	14.1	(Krau3) (6V00	μs
Φm	Phase margin at unity gain	RL = 50 kه,	CL = 100 pF‡	25°C	- 0V	63°	(enatric	this tuol	63°	Bucch East	.00
	Gain margin		-	25°C		14			14	1-11-11	dB

[†] Full range is – 40°C to 85°C. [‡] Referenced to 2.5 V



Second Second	PARAMETER	TEOT	CONDITIONS	TLV2264Y		UNIT
TIME	PARAMETER	IESI	CONDITIONS	MIN TYP	MAX	UNIT
VIO	Input offset voltage	25*0 9.35		300	2500	μV
10	Input offset current	$V_{DD\pm} = \pm 1.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ $R_S = 50 \Omega$	0.5	150	pА
IB	Input bias current	v0=0,	115 = 00 22	1	150	pА
VICR	Common-mode input voltage range	V _{IO} ≤5 mV,	R _S = 50 Ω	0 -0.3 to to 2 2.2	Equiv salon	V
	Likely lovel as dead wellings	I _{OH} = -20 µA	sin 1 6i s	2.99	and the second second	
VOH	High-level output voltage	I _{OH} = -200 µA	sta 10 Hz	2.7 2.75	98ion	V
		V _{IC} = 0,	l _{OL} = 50 μA	10	vie staril	
VOL	Low-level output voltage	V _{IC} = 0,	I _{OL} = 500 μA	100	125	V
		V _{IC} = 0,	I _{OL} = 1 mA	200	250	
A	Large-signal differential	No AND ON	$R_L = 50 k\Omega^{\dagger}$	60 100	NOTERIO I	
AVD	voltage amplification	$V_{O} = 1 V \text{ to } 2 V$	$R_L = 1 M\Omega^{\dagger}$	100	291211	V/m\
rid	Differential input resistance	0*82	12, UC = 391	1012	million -	Ω
ri	Common-mode input resistance			1012		Ω
ci	Common-mode input capacitance	f = 10 kHz	and the second s	8	10.548	pF
zo	Closed-loop output impedance	f = 100 kHz,	Ay = 10	270	-	Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 1.7 V,	$V_{O} = 0$, $R_{S} = 50$	Q 65 77		dB
KSVR	Supply voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	$V_{DD} = 2.7 V \text{ to } 8 V,$	No load, $V_{IC} = 0$	80 100		dB
IDD	Supply current (four amplifiers)	$V_{O} = 0,$	No load	0.8	1	mA

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

† Full range is ~ 40°C to 85°C ¥ Referenced to 2.5 V



	DADAMETER	TEOT	CONDITIONS	TI	LV22641	1	UNIT
	PARAMETER	IEST	CONDITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage				300	2500	μV
10	Input offset current	$V_{DD\pm} = \pm 2.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ $R_S = 50 \Omega$		0.5	150	pА
IB	Input bias current		HS = 50 22	and a	1	150	pА
VICR	Common-mode input voltage range	V _{IO} ≤5 mV,	R _S = 50 Ω	0 to 4	-0.3 to 4.2		v
		I _{OH} = -20 µA	vollage	uqui 🦳	4.99	/	
VOH	High-level output voltage	I _{OH} = -100 μA		4.85	4.94	-	V
		I _{OH} = -200 μA	alexies index over	4.7	4.85	-	
	The second secon	V _{IC} = 2.5 V,	loL = 50 μA		0.01	-	
VOL	Low-level output voltage	V _{IC} = 2.5 V,	ΙΟΓ = 200 πγ		0.09	0.15	V
	Providence and the second seco	V _{IC} = 2.5 V,	I _{OL} = 1 mA	sho	0.2	0.3	
A	Large-signal differential	VIC = 2.5 V,	$R_L = 50 k\Omega^{\dagger}$	80	170	-	1//>
AVD	voltage amplification	$V_0 = 1 V \text{ to } 4 V$	$R_L = 1 M\Omega^{\dagger}$	-	550	-	V/m\
rid	Differential input resistance		and an it is a sub-track to be the	ing	1012		Ω
rj	Common-mode input resistance	in the second second			1012		Ω
ci	Common-mode input capacitance	f = 10 kHz	and the second	1.0	8	-	pF
zo	Closed-loop output impedance	f = 100 kHz,	Ay = 10	n	240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V,	$V_{O} = 2.5 V$, $R_{S} = 50 \Omega$	70	83		dB
ksvr	Supply voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	V _{DD} = 4.4 V to 8 V,	No load, $V_{IC} = V_{DD}/2$	80	95	*	dB
IDD	Supply current (four amplifiers)	$V_{O} = 2.5 V_{1}$	No load		0.8	1	mA

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

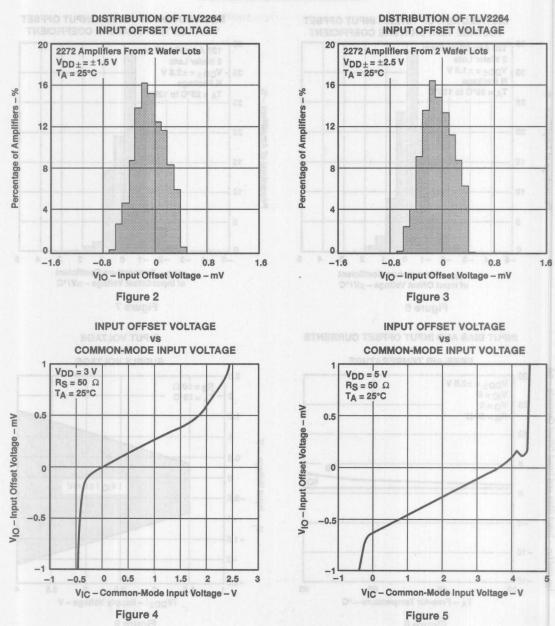
† Referenced to 2.5 V



	Table of Gra	phs	PARAMETE
008			FIGURE
VIO	Input offset voltage	Distribution	2,3
	Input offset voltage	vs Common-mode voltage	4,5 *
ανιο	Input offset voltage temperature coefficient	Distribution	6,7
IIB/IIO	Input bias and input offset currents	vs Free-air temperature	8
VI	Include the second s	vs Supply voltage	9
	Input voltage	vs Free-air temperature	10
VOH	High-level output voltage	vs High-level output current	11, 14
VOL	Low-level output voltage	vs Low-level output current	12, 13, 15
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	16
1	Short aircuit autout auroant	vs Supply voltage	17
los	Short-circuit output current	vs Free-air temperature	18
VID	Differential input voltage	vs Output voltage	19, 20
AVD	and a second	vs Load resistance	21
	Differential voltage amplification	vs Frequency	22, 23
		vs Free-air temperature	24, 25
zo	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency	28
		vs Free-air temperature	29
k _{SVR} Su	Supply-voltage rejection ratio	vs Frequency	30, 31
		vs Free-air temperature	32
IDD	Supply current	vs Free-air temperature	33
SR	Slew rate	vs Load capacitance	34
Sh		vs Free-air temperature	35
Vo	Large-signal pulse response	vs Time	36, 37, 38, 39
Vo	Small-signal pulse response	vs Time	40, 41, 42, 43
V'n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage (referred to input)	Over a 10-second period	46
	Integrated noise voltage	vs Frequency	47
THD + N	Total harmonic distortion plus noise	vs Frequency	48
	Gain-bandwidth product	vs Free-air temperature	49
		vs Supply voltage	50
φm	Phase margin	vs Frequency	22, 23
	i nase nalgin	vs Load capacitance	51
	Gain margin	vs Load capacitance	52
B ₁	Unity-gain bandwidth	vs Load capacitance	53
Card Internet	Overestimation of phase margin	vs Load capacitance	54



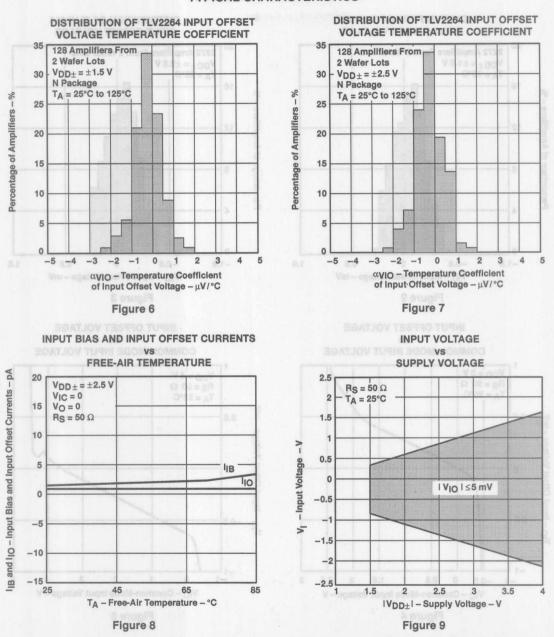
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TYPICAL CHARACTERISTICS[†]

[†] For all curves where VDD = 5 V, all loads are referenced to 2.5 V. For all curves where VDD = 3 V, all loads are referenced to 1.5 V.

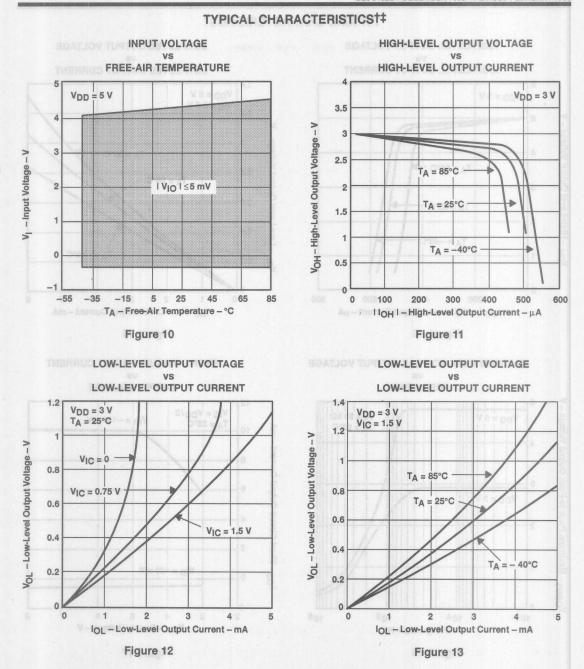




TYPICAL CHARACTERISTICS[†]

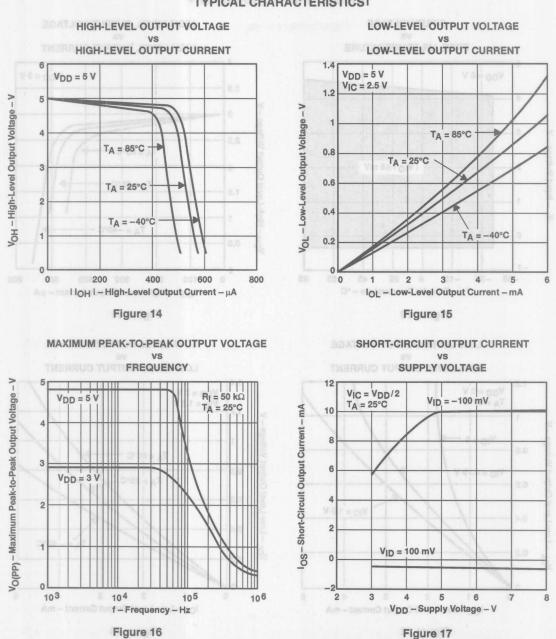
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





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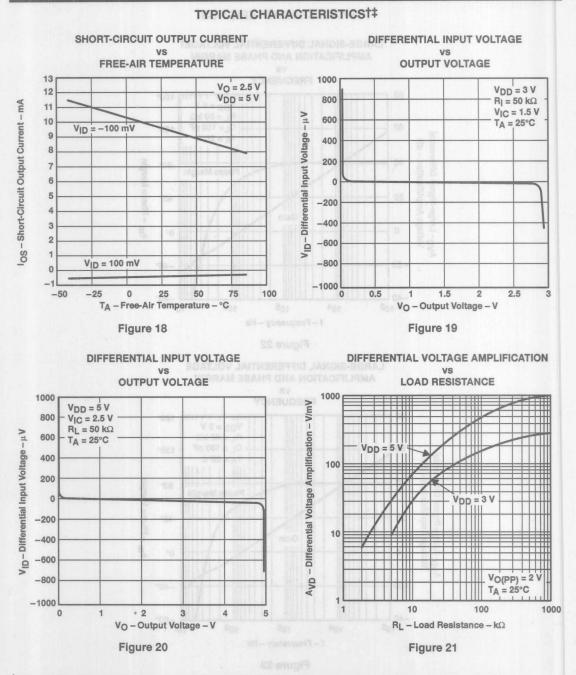




TYPICAL CHARACTERISTICS†

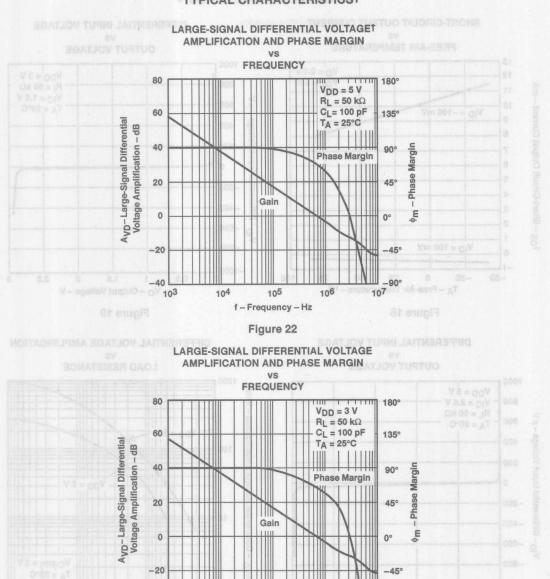
[†] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.





[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.





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TYPICAL CHARACTERISTICS[†]

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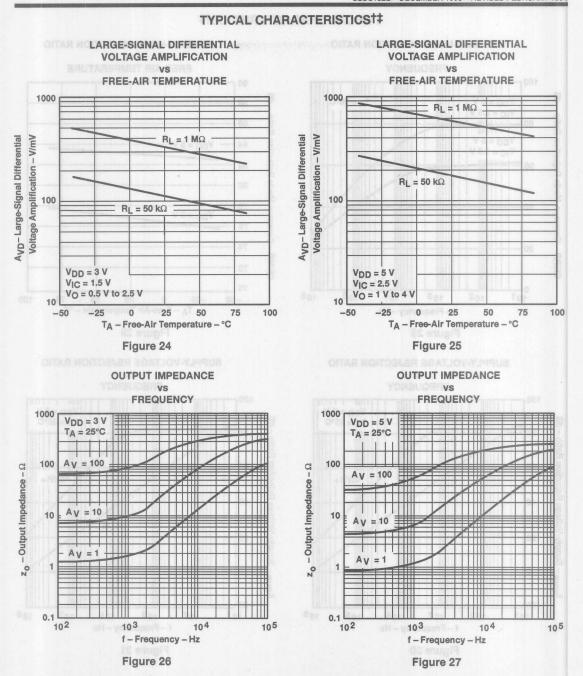
f – Frequency – Hz Figure 23

INSTRUMENTS

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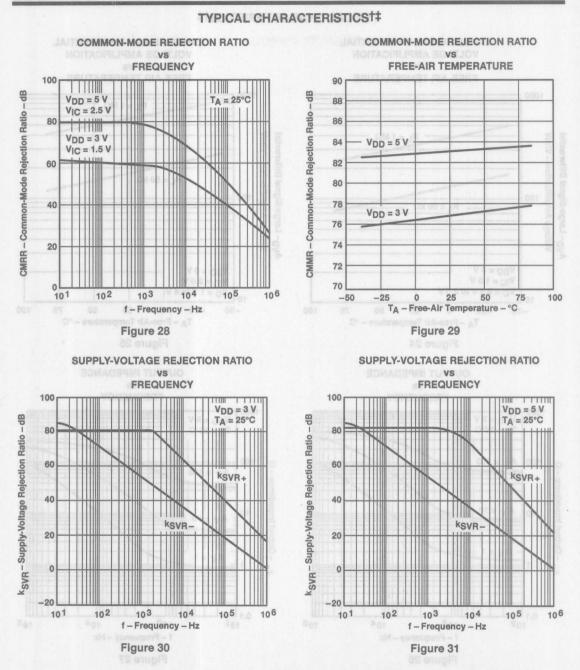
[†] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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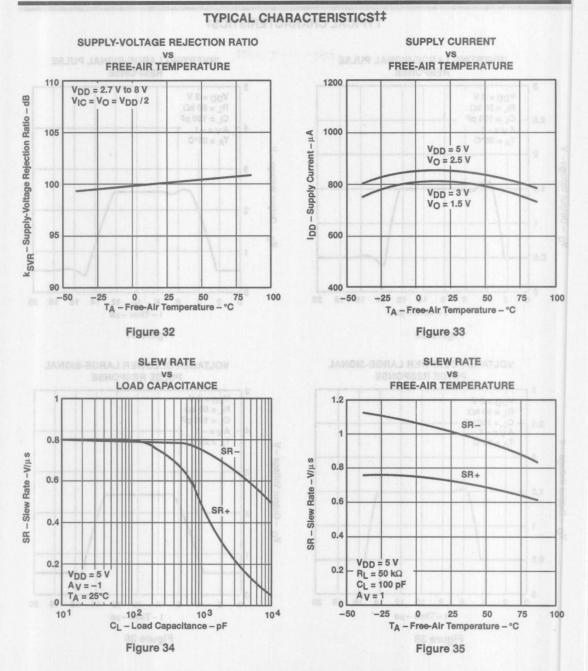
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where $V_{DD} = 5 V$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 V$, all loads are referenced to 1.5 V.





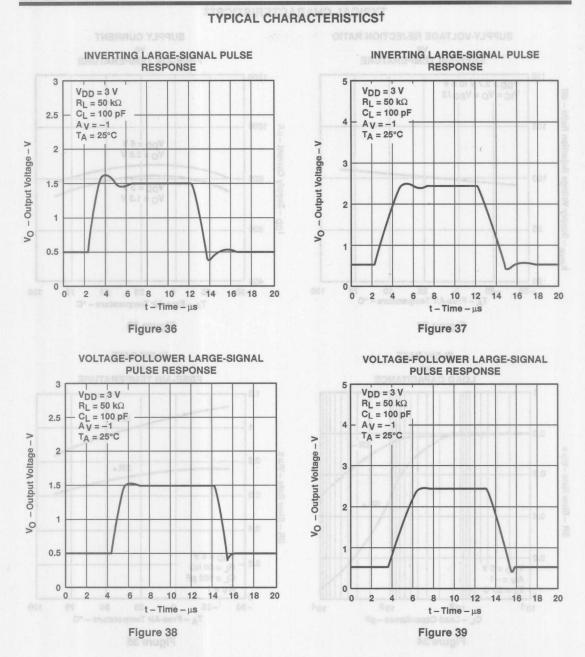
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.





[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where $V_{DD} = 5 V$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 V$, all loads are referenced to 1.5 V.



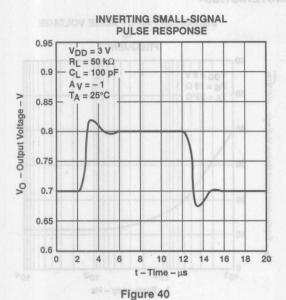


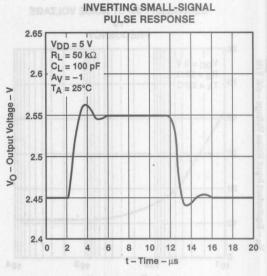
[†] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.



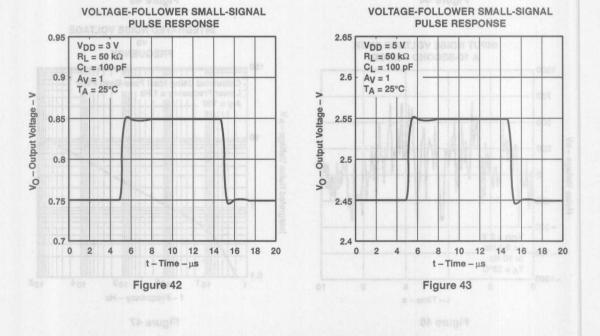
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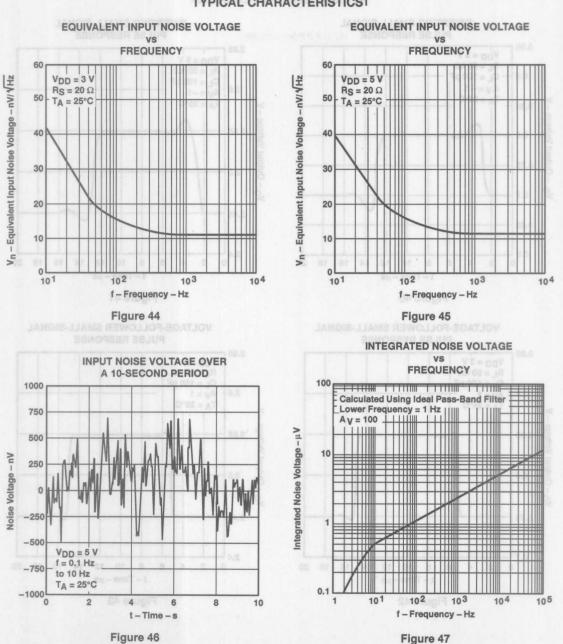






† For all curves where VDD = 5 V, all loads are referenced to 2.5 V. For all curves where VDD = 3 V, all loads are referenced to 1.5 V.

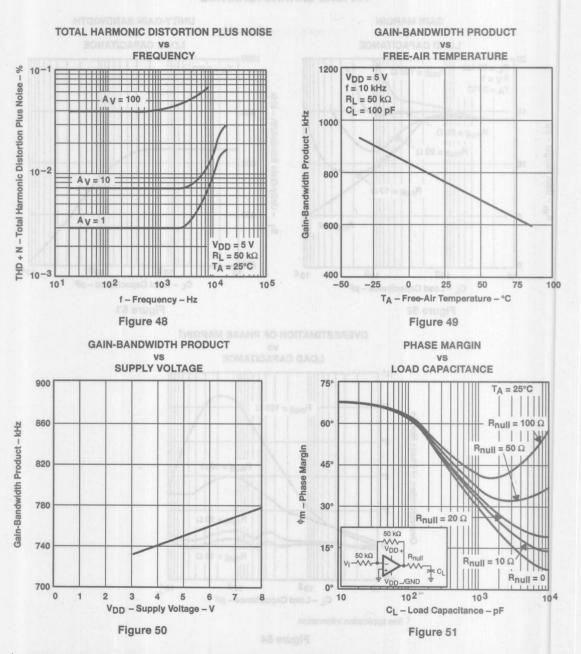




TYPICAL CHARACTERISTICS[†]

[†] For all curves where VDD = 5 V, all loads are referenced to 2.5 V. For all curves where VDD = 3 V, all loads are referenced to 1.5 V.

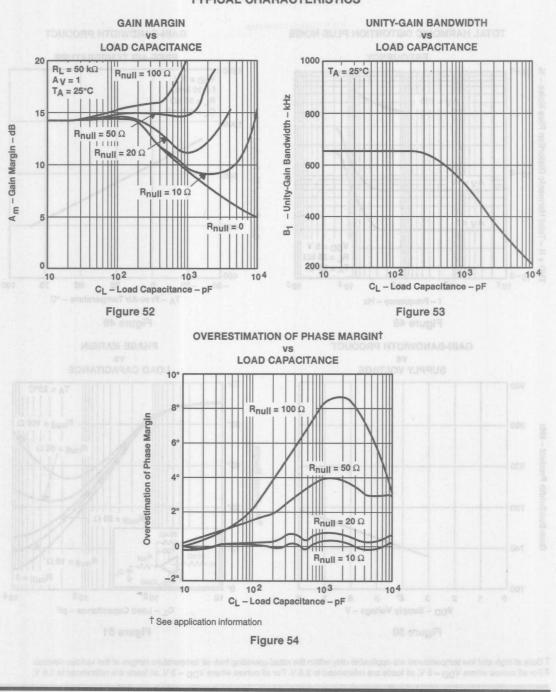




TYPICAL CHARACTERISTICS^{†‡}

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. [‡] For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.





TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

loading considerations

The TLV2264 is a low-voltage, low-power version of the TLC2274 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2264 is similar to the TLC2274 and is capable of driving several milliamperes.

The design topology used for the TLV2264 or the TLC2274 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. While the TLC2274 is capable of greater than 1-mA drive from the positive rail, the TLV2264 is capable of only a few hundred microamperes. When designing with lower impedance loads (less than 50 k Ω) with the TLV2264, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2264 topology provides lower drive to the positive rail than other high-output-drive rail-to-rail operational amplifiers, it is a more stable topology.

driving large capacitive loads

The TLV2264 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω , 20 Ω , 50 Ω , and 100 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta \theta_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times \text{R}_{\text{null}} \times \text{C}_{\text{I}} \right)$$

where : $\Delta \theta_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

 $C_1 = load capacitance$

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$= \frac{1}{1 + g_m \times R_{null}}$$

(2)

(1)

where : F = factor reducing frequency of pole

 $g_m = \text{small-signal output transconductance (typically 4.83 \times 10^{-3} \text{ mhos})}$

 R_{null} = output series resistance



TLV2264, TLV2264A, TLV2264Y Advanced LinCMOSTM RAIL-TO-RAIL QUAD OPERATIONAL AMPLIFIERS SLOS132B - DECEMBER 1993 - REVISED FEBRUARY 1994

APPLICATION INFORMATION

driving large capacitive loads (continued)

For the TLV2264, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L : at $C_L = 10$ pF, use 60 MHz, at $C_L = 1000$ pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation (1) to better approximate the improvement in phase margin.

$$\Delta \theta_{m2} = \tan^{-1} \left[\frac{UGBW}{(F \times P_2)} \right] - \tan^{-1} \left(\frac{UGBW}{P_2} \right)$$

where : $\Delta \theta_{m2}$ = reduction in phase margin

and been UGBW = unity-gain bandwidth frequency

- F = factor from equation (2)
- P₂ = unadjusted pole (60 MHz @ 10 pF, 6 MHz @ 100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

 $V_{I} \xrightarrow{50 \text{ k}\Omega} V_{DD+}$ F_{null} $F_{DD-/GND} \xrightarrow{CL}$ Figure 55. Series-Resistance Circuit

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To real equation (1), UGBW must be aboroximated from Figure 53.

Using equation (1) atone overestinates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

(3)

here : F = factor reducing frequency of pole .

or. = small-signal output transconductance (typically 4.83 x 10⁻² minos)

- entroite series resistance -



APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using $PSpice^{\textcircled{m}}$ PartsTM model generation software. The Boyle macromodel and subcircuit in Figure 56 are generated using the TLV2264 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

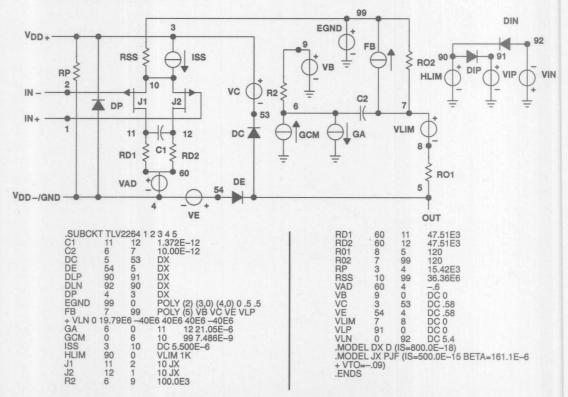


Figure 56. Boyle Macromodel and Subcircuit

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APPLICATION INFORMATION

nacromodal Information

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lacromodel information provided is derived using PSpice[®] Parts[®] model generation software. The Boyle tacromodel and subcircuit in Figure 56 are geneyated using the TLV2264 typical electrical and operating haracteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be enerated to a tolerance of 20% (in most cases):

- priva epallov tuqtuo evitiaoq mumixaM
 - Maximum nedative output voltage
 - Siew mate
 - Quiescent power dissipation
 - Open-loop voltage amplification

- Unity-gain frequency
- Common-moda rejection ratio
 - Phase margin
 - DC output resistan
 - AC outout resistance
- Short-circuit output dumant limit



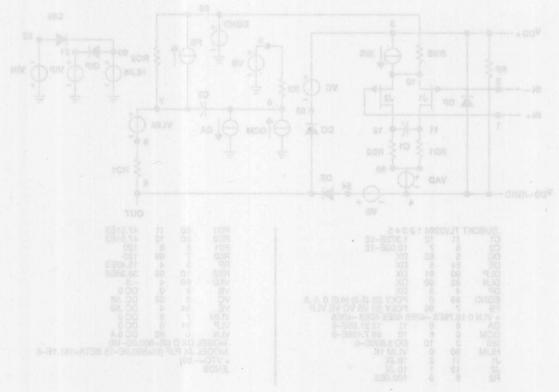


Figure 55, Boyle Macromodel and Suborrout

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(TOP VIEW)

- Wide Range of Supply Voltages Over Specified Temperature Range: $T_A = -40^{\circ}C$ to 85°C...2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10¹² Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

description

The TLV2322 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low-power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27 μ A over its full temperature range of -40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments

silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

VAI	LAB	LE	OPT	TIONS

		PAC	KAGED DEVICE	S	
TA	VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
-40°C to 85°C	9 mV	TLV2322ID	TLV2322IP	TLV2322IPWLE	TLV2322Y

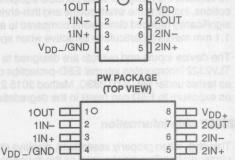
The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2322IDR). The PW package is only available left-end taped and reeled (e.g., TLV2322IPWLE).

A

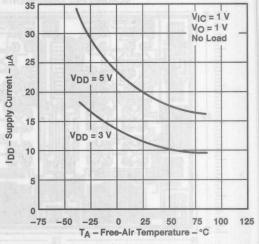
LinCMOS™ is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.





SUPPLY CURRENT vs FREE-AIR TEMPERATURE



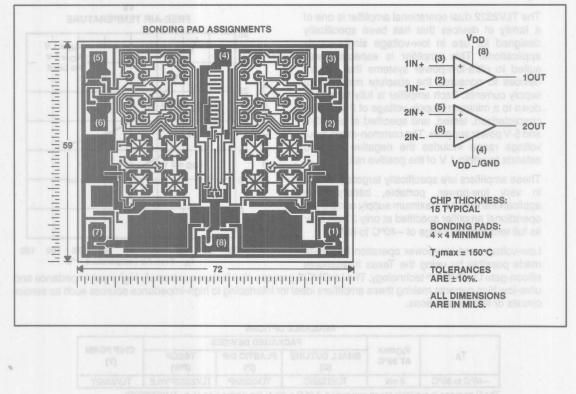
description (continued)

To facilitate the design of small portable equipment, the TLV2322 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2322 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD can result in the degradation of the device parametric performance.

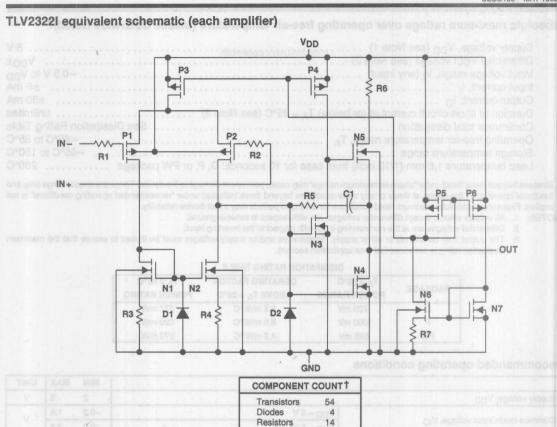
TLV2322Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2322I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



The Di package is evaluate tabled and reased, and humin to the davide type (p.g., Ft. The RM reasons is enty available Mitmane Latert and realed (e.g., T1/102200034 E).

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† Includes both, amplifiers and all ESD, bias, and trim circuitry

2

Capacitors



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1)	8 V
Differential input voltage (see Note 2)	
Input voltage range, V _I (any input)	
Input current, I	
Output current, Io	±30 mA
Duration of short-circuit current at (or below) T _A = 25°C (see Note 3)	
Continuous total dissipation	
Operating free-air temperature range, TA	
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW p	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

	DISSIPAT	TION RATING TABLE	
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
D	725 mV	5.8 mW/°C	377 mW
P	1000 mV	8.0 mW/°C	520 mW
PW	525 mV	4.2 mW/°C	273 mW

recommended operating conditions

in the second	COMPOSIENT COUNTY	MIN	MAX	UNIT
Supply voltage, VDD	Transistore 50	2	8	V
Common-mode input voltage, V _{IC} $V_{DD} = 3 V$ $V_{DD} = 5 V$	V _{DD} = 3 V	-0.2	1.8	.8
	V _{DD} = 5 V	-0.2	3.8	V
Operating free-air temperature, TA	because of the second se	-40	85	°C

to mite bran, exite, GBB line



	isesou it			TLV23			3221			
	PARAMETER	TEST CONDITIONS	TAT	V	DD = 3 \	/	V	DD = 5 \	1	UNIT
	Viewment	V.F.	MIN	TYP	MAX	MIN	TYP	MAX	1	
	50:0 Ora	$V_{O} = 1 V,$ $V_{IC} = 1 V,$	25°C	- 191 	1.1	9	also vitn	1.1	9	mV
VIO	Input offset voltage	$R_{S} = 50 \Omega,$ $R_{L} = 1 M\Omega$	Full range	1 = 1 #18		11	s alon tu	alert ing	11	mv
ανιο	Average temperature coefficient of input offset voltage	QL = 28 gR Bea Figure 30	25°C to 85°C	VOV JR	1	lwbnad	yrikan tuk	1.1	Maxim	μV/°C
1.194	Input effect surrent (coo Note 4)	V _O = 1 V,	25°C	= IV	0.1		distant	0.1	and and a	pA
IIO	Input offset current (see Note 4)	VIC = 1 V	85°C	221	22	1000		24	1000	рА
IIB	Input bias current (see Note 4)	V _O = 1 V,	25°C	= įV	0.6			0.6		pA
IB		VIC = 1 V	85°C	12	175	2000		200	2000	pri
	Common-mode input	e aaV .etutetee	25°C	-0.2 to 2	-0.3 to 2.3	a fe e	-0.2 to 4	-0.3 to 4.2	la nei	V
VICR	voltage range (see Note 5)	enoma	Full range	-0.2 to 1.8			-0.2 to 3.8	NR MA		v
	60.0	V _{IC} = 1 V,	25°C	1.75	1.9		3.2	3.8		
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $I_{OH} = -1 \text{ mA}$	Full range	1.7			3	u ta dilar	WE(C	V
	510 0.02	V _{IC} = 1 V,	25°C	569	115	150		95	150	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	L=1		190	ut noise	onitheir	190	mV
	Large-signal differential	VIC = 1 V,	25°C	50	400		50	520		
AVD	voltage amplification	R _L = 1 MΩ, See Note 6	Full range	50	THE	NWONBO	50	into unita	TOCETVA:	V/m\
CMRR	Common-mode rejection ratio	$V_{O} = 1 V$, $V_{IC} = V_{ICR} min$,	25°C	65	88		65	94	VinU	dB
CIVILUT	Common mode rejection ratio	$R_{\rm S} = 50 \ \Omega$	Full range	60			60			GD
ksvr	Supply-voltage rejection ratio	$V_{IC} = 1 V, V_{O} = 1 V,$	25°C	70	86		70	86	Phase	dB
SVR	(ΔVDD/ΔVIO)	R _S = 50 Ω	Full range	65			65			UB
	Supply current	$V_{O} = 1 V, V_{IC} = 1 V,$	25°C		12	34		20	34	μА
DD	Coppy current	No load	Full range			54			54	μΑ

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically. 5. This range also applies to each input individually.

6. At VDD = 5 V, VO(PP) = 0.25 V to 2 V; at VDD = 3 V, VO = 0.5 V to 1.5



	DADAMETED	TEOTO		-	TLV23221	UNIT	
	PARAMETER	TEST CO	ONDITIONS	TA	MIN TYP MAX		
SR		$V_{IC} = 1 V,$	$V_{I(PP)} = 1 V,$	25°C	0.02	Mue	
24	Siew rate at unity gain	$R_{L} = 1 M\Omega_{2}, \qquad C_{L} = 20 \text{ pr},$ See Figure 30	Slew rate at unity gain $R_L = 1 M\Omega$, $C_L = 20 pF$, See Figure 30		85°C	0.02	- V/μs
v _n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	68	nV/√Hz	
Pour	Maximum output swing bandwidth	Vo = VoH,	CL = 20 pF,	25°C	2.5	kHz	
BOM	Maximum output swing bandwidth		See Figure 30	85°C	equation tes 2 hught to		
D.	Unity-gain bandwidth	V _I = 10 mV,	CL = 20 pF,	25°C	27	lal la	
B ₁	Onity-gain bandwidth	$R_L = 1 M\Omega$, See Figure 3	$R_L = 1 M\Omega$, See Figure 32	See Figure 32	85°C	21	- kHz
THE STREET CO.	8.0 8.0	V _I = 10 mV,	f= B1,	-40°C	39°		
φm	Phase margin	CL = 20 pF,	R _L = 1 MΩ,	25°C	34°	60	
		See Figure 32		85°C	28°	1	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

TLV23221 PARAMETER **TEST CONDITIONS** TA UNIT MIN TYP MAX 25°C 0.03
$$\label{eq:VIC} \begin{split} V_{IC} &= 1 \ V, \\ R_L &= 1 \ M\Omega, \\ C_L &= 20 \ pF, \end{split}$$
 $V_{I(PP)} = 1 V$ 85°C 0.03 SR Slew rate at unity gain V/µs 25°C 0.03 $V_{I(PP)} = 2.5 V$ See Figure 30 85°C 0.02 f = 1 kHz, $R_S = 100 \Omega$, Vn Equivalent input noise voltage 25°C 68 nV/√Hz See Figure 31 25°C 5 $C_{I} = 20 \, pF$, VO = VOH, BOM Maximum output swing bandwidth kHz $R_L = 1 M\Omega$, See Figure 30 85°C 4 25°C 85 $V_{I} = 10 \text{ mV},$ $C_{L} = 20 \, \text{pF},$ Unity-gain bandwidth B1 kHz See Figure 32 $R_L = 1 M\Omega$, 85°C 55 -40°C 38° f = B₁, $V_{I} = 10 \text{ mV},$ $R_L = 1 M\Omega$, Phase margin $C_{L} = 20 \, pF$, 25°C φm 34° See Figure 32 85°C 28°

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Tes: 4. The typical values of input bias ourrent and input offset ourrent batow 5 pA are determined malifemation

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	electrical	characteristics,	TA	= 25°C
--	------------	------------------	----	--------

					TLV23	322Y			
	PARAMETER	TEST CONDITIONS	V	DD = 3 \	/	V _{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage			1.1	9	y textito t	1.1	9	mV
10	Input offset current (see Note 4)	V _O = 1 V, V _{IC} = 1 V		0.1			0.1	No.	pА
IIB	Input bias current (see Note 4)	V _O = 1 V, V _{IC} = 1 V		0.6	and the second	in Inner	0.6		pА
VICR	Common-mode input voltage range (see Note 5)	ve Terrovrove	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		v
VOH	High-level output voltage	$V_{IC} = 1 V$, $V_{ID} = -100 mV$, $I_{OH} = -1 mA$	1.75	1.9	silov luc	3.2	3.8	JOY	V
VOL	Low-level output voltage	$V_{IC} = 1 V$, $V_{ID} = 100 mV$, $I_{OL} = 1 mA$		115	150		95	150	mV
AVD	Large-signal differential voltage amplification	$V_{IC} = 1 V$, $R_L = 1 M\Omega$, See Note 6	50	400		50	520	CVA 	V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V, V_{IC} = V_{ICR} min,$ R _S = 50 Ω	65	88	turni eb	65	94	VIC	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD} / \Delta V_{ID})$	$V_{O} = 1 V,$ $V_{IC} = 1 V,$ Rs = 50 Ω	70	86	î.	70	86	681	dB
IDD	Supply current	V _O = 1 V, V _{IC} = 1 V, No load		12	34	eter	20	34	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

	aganoryadda	

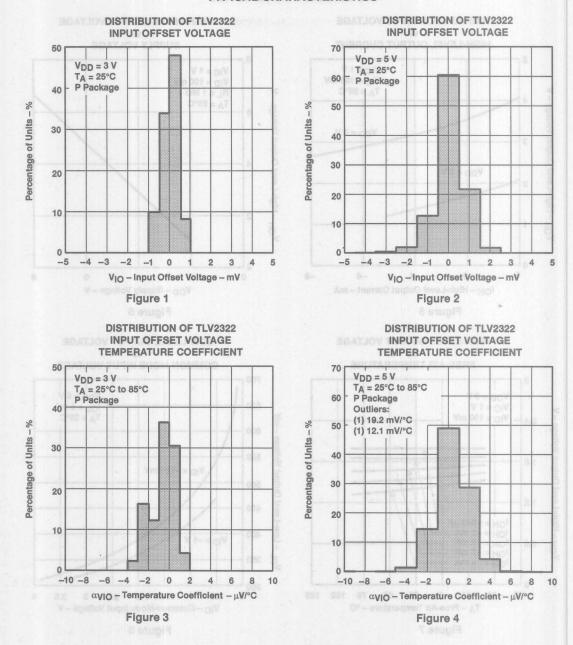


8.54 C	IND. TPP MAX MIN TYP		FIGURE
VIO	Input offset voltage	Distribution	1,2
VIO	Input offset voltage temperature coefficient	Distribution	3, 4
	10	vs Output current	5
VOH	High-level output voltage	vs Supply voltage	6
	-0.2 -0.2 -0.	vs Temperature	7
3	2 23 4 41	vs Common-mode input voltage	8
10.	Low-level output voltage	vs Temperature	9, 11
VOL	Low-level output voltage	vs Differential input voltage	10
		vs Low-level output current	12
		vs Supply voltage	13
AVD	Large-signal differential voltage amplification	vs Temperature	14
IB/IIO	Input bias and offset currents	vs Temperature	15
/IC	Common-mode input voltage	vs Supply voltage	16
	Supply current	vs Supply voltage	17
DD	Supply current	vs Temperature	18
SR	Slew rate	vs Supply voltage	19
on.	Siew rate	vs Temperature	20
O(PP)	Maximum peak-to-peak output voltage	vs Frequency	21
	Unity-gain bandwidth	vs Temperature	22
31	Unity-gain bandwidth	vs Supply voltage	23
AVD	Large-signal differential voltage amplification	vs Frequency	24, 25
		vs Supply voltage	26
m	Phase margin	vs Temperature	27
		vs Load capacitance	28
/n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

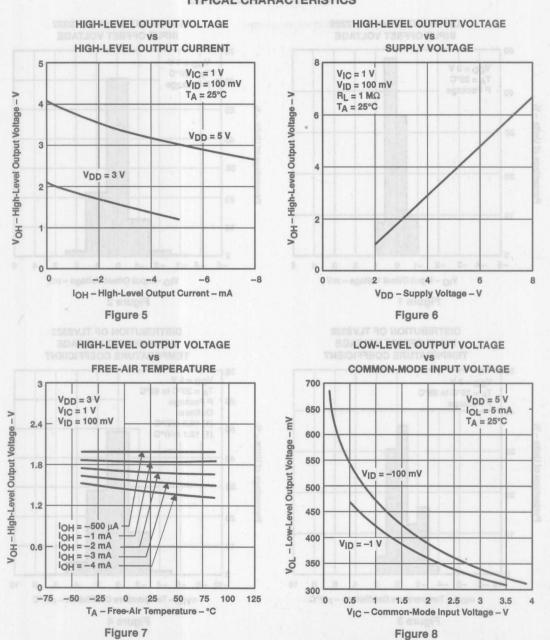
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



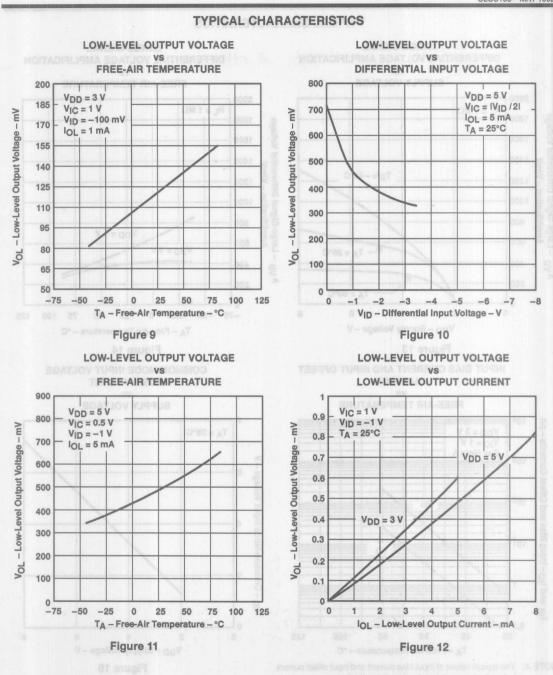




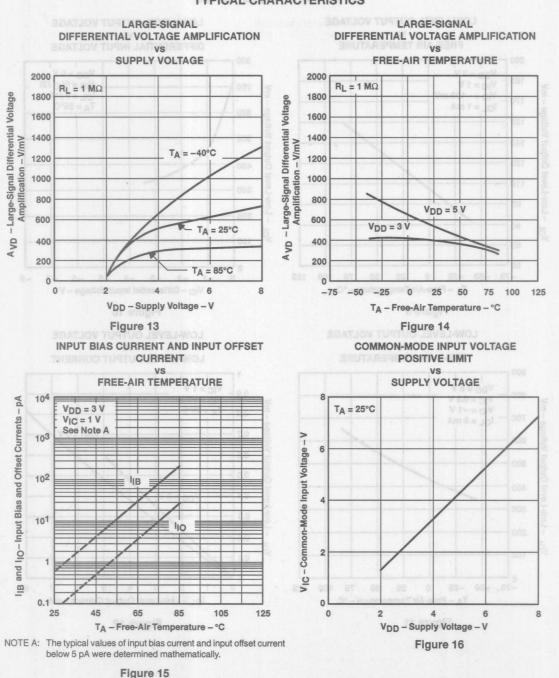
TYPICAL CHARACTERISTICS



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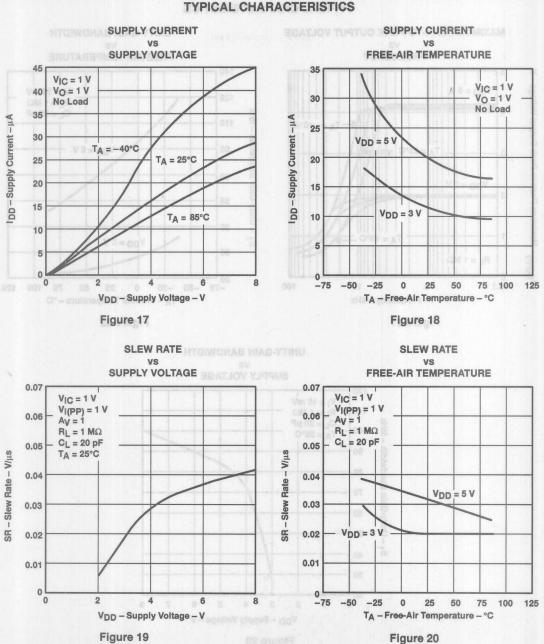
TYPICAL CHARACTERISTICS

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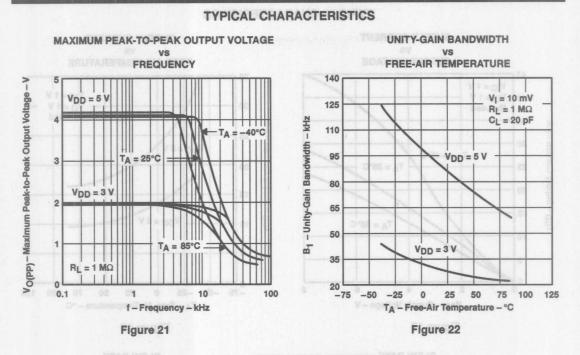
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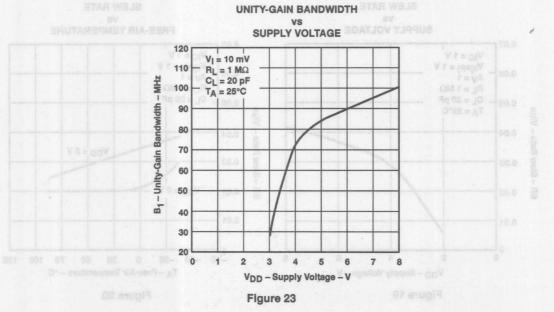
LinCMOS™ LOW-VOLTAGE LOW-POWER DUAL OPERATIONAL AMPLIFIERS SLOS109 - MAY 1992











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TYPICAL CHARACTERISTICS

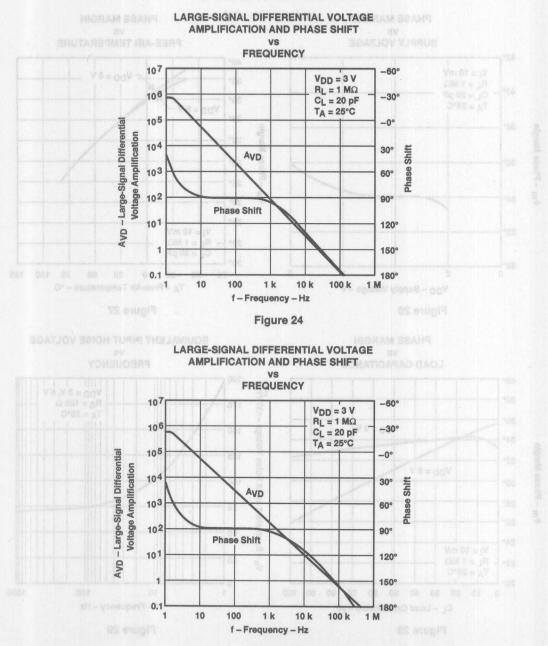
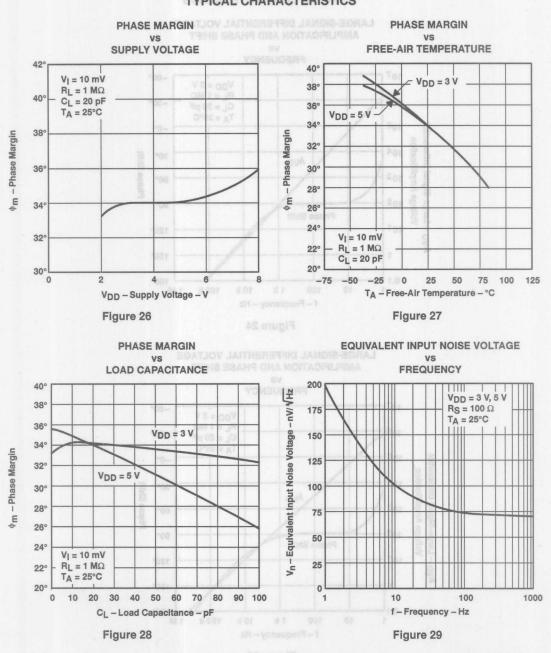


Figure 25



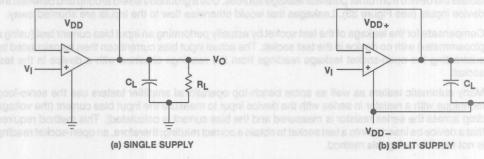
TYPICAL CHARACTERISTICS

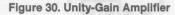


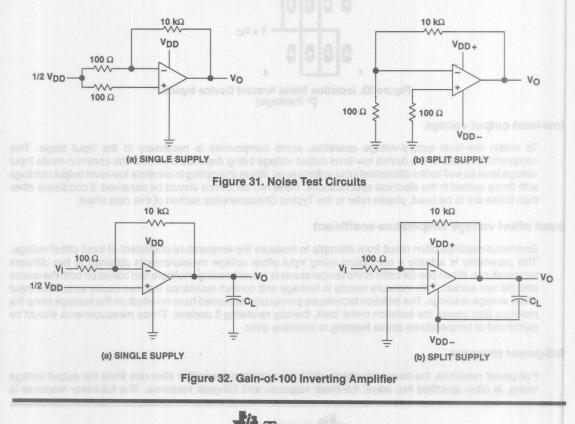
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2322 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.







2-79

Vo

< RL

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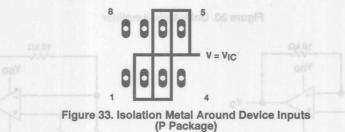
PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2322 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a
 picoammeter) with no device in the test socket. The actual input bias current can then be calculated by
 subtracting the open-socket leakage readings from the readings obtained with a device in the test
 socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.



low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

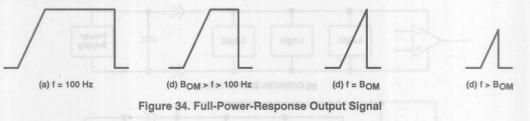
Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is



PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2322 performs well using dualpower supplies (also called balanced or split supplies), the design is optimized for singlesupply operation. This includes an input commonmode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to V_{DD}/2, while consuming very little power and is suitable for supply voltages of greater than 4 V.

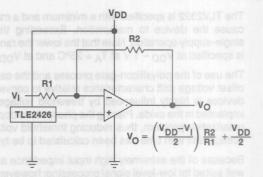


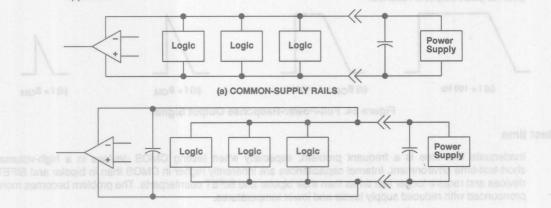
Figure 35. Inverting Amplifier With Voltage Reference



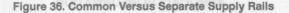
APPLICATION INFORMATION

single-supply operation (continued)

- The TLV2322 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:
 - Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
 - Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive
 decoupling is often adequate; however, RC decoupling may be necessary in high-frequency
 applications.



(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)



input characteristics

ngle-supply operation

The TLV2322 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

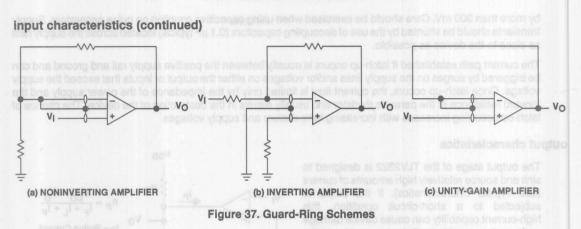
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2322 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2322 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



APPLICATION INFORMATION



noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2322 result in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

electrostatic-discharge protection

The TLV2322 incorporates an internal electrostatic-discharge (ESD)-protection circuit

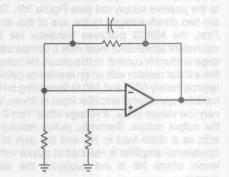


Figure 38. Compensation for Input Capacitance

that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD can result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2322 inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage



APPLICATION INFORMATION

by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2322 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2322 possesses excellent high-level output voltage and current capability methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2322 are measured using a 20-pF load. The device drives

VDD VI \downarrow $R_{P} = \frac{V_{DD} - V_{O}}{I_{F} + I_{L} + I_{P}}$ $I_{P} = Pullup Current$ Required by the Operational Amplifier (typically 500 µA)

Figure 39. Resistive Pullup to Increase VOH

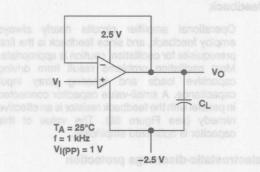


Figure 40. Test Circuit for Output Characteristics

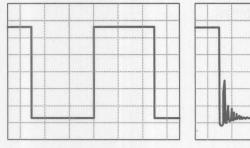
higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

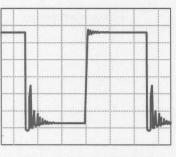
Because CMDS devices are sustaptible to latch-up due to their initiatent gatas lig try rations, the TLV3322 inputs and outputs are designed to withstand ~100-mA surge ourrents without sustaining latch-up; however, tectiniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be to word biasest. Applied input and output voltage should not exceed the supply voltage

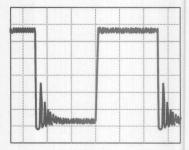


APPLICATION INFORMATION









(a) $C_L = 20 \text{ pF}$, $R_L = \text{NO LOAD}$ (b) $C_L = 260 \text{ pF}$, $R_L = \text{NO LOAD}$

(c) $C_L = 310 \text{ pF}$, $R_L = \text{NO LOAD}$

Figure 41. Effect of Capacitive Loads



TLV23221, TLV23221, TLV23221 LincmosTM LOW-VOLTAGE LOW-POWER DUAL OPERATIONAL AMPLIFIERS

APPLICATION NEORMATION

C1 = 20 pF, R1 = 110 LOAD

and the second second second second

igure 41. Effect of Capacitive Loads

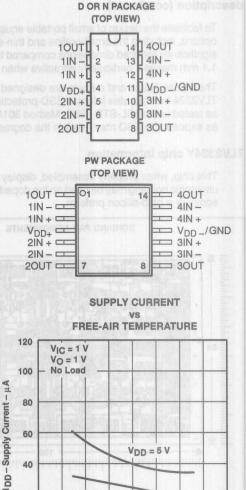
- Wide Range of Supply Voltages Over **Specified Temperature Range:** $T_A = -40^{\circ}C$ to $85^{\circ}C...2$ V to 8 V
- Fully Characterized at 3 V and 5 V
- -Single-Supply Operation
- **Common-Mode Input-Voltage Range** Extends Below the Negative Rail and up to Vpp -1 V at 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10¹² Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

description

The TLV2324 guad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier is specified at only 27 µA over its full temperature range of -40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate, LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making them ideal for interfacing to highimpedance sources such as in sensor circuits or filter applications.



VDD = 3 V 20 0 -75 -50 -25 0 25 50 75 100 125 TA - Free-Air Temperature - °C

AVAI	LABLE	OPT	IONS
------	-------	-----	------

	PACKAGED DEVICES					
TA	VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP TSSOP (N) (PW)		CHIP FORM (Y)	
-40°C to 85°C	10 mV	TLV2324ID	TLV2324IN	TLV2324IPWLE	TLV2324Y	

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2324IDR). The PW package is only available left-end taped and reeled (e.g., TLV2324IPWLE).

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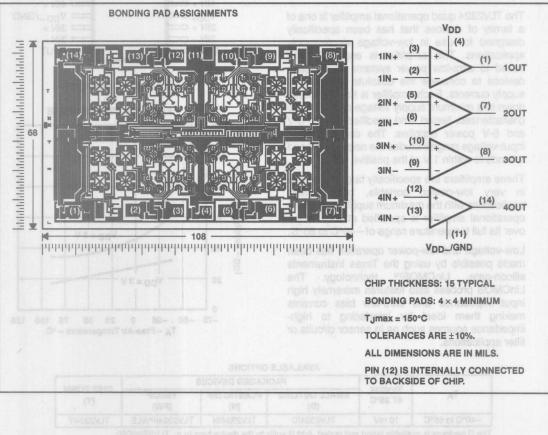
description (continued)

To facilitate the design of small portable equipment, the TLV2324 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline package (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2324 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

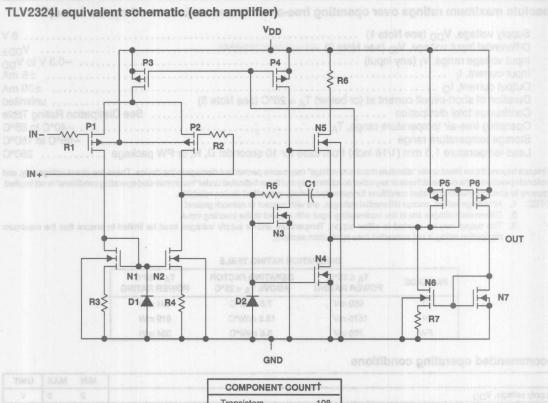
TLV2324Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2324I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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	COMPONENT COUN	TT	way and a second s
	Transistors	108	
	Diodes	8	
	Resistors	28	
	Capacitors	4	
	Tincludes all amplifiers	ESD	

bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{DD} (see Note 1) 8 V Differential input voltage, V _{ID} (see Note 2) $V_{DD\pm}$ Input voltage range, V _I (any input) -0.3 V to V _{DD} Input current, I ₁ ± 5 mA Output current, I ₀ ± 30 mA Duration of short-circuit current at (or below) T _A = 25°C (see Note 3) unlimited See Dissipation Bating Table See Dissipation Bating Table
Continuous total dissipation
Operating free-air temperature range, T _A
Storage temperature range65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground. 2. Differential voltages are at the noninverting input with respect to the inverting input.

 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE						
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING			
D	950 mV	7.6 mW/°C	494 mW			
N	1575 mV	12.6 mW/°C	819 mW			
PW	700 mV	5.6 mW/°C	364 mW			

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, VDD	A CANADA AND AND A CANADA AND AND A CANADA AND AND AND AND AND AND AND AND AN	2	8	V
	V _{DD} = 3 V	-0.2	1.8	V
Common-mode input voltage, VIC	V _{DD} = 5 V	-0.2	3.8	V
Operating free-air temperature, TA	C. te orangeo d	-40	85	°C



	TEV2824	TEST CONDITIONS		TLV2324I						
	PARAMETER		TAT	V _{DD} = 3 V		/	V _{DD} = 5 V		1	UNIT
0.02		V((PP) = 1 V)	,V ? =	MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	$V_{O} = 1 V,$ $V_{IC} = 1 V,$	25°C	4U.4 (3eo	1.1	10	nise var	1.1	10	mV
VIO	input onset voltage	$R_S = 50 \Omega$, $R_L = 1 M\Omega$	Full range	(=) 895		12	ealon tu	qni Insla	12	n
αVIO	Average temperature coefficient of input offset voltage	OL ≈ 20 pF; See Figure 30	25°C to 85°C	OV A	1	iwbried	ang ang ang	1.1	Maxin	μV/°C
	Innut offerst summert (and Note 4)	V _O = 1 V,	25°C	+NE	0.1			0.1		pA
10	Input offset current (see Note 4)	$V_{IC} = 1 V$	85°C	a jā	22	1000	CUO PRO	24	1000	рА
IIB	Input bias current (see Note 4)	V _O = 1 V,	25°C	-W	0.6			0.6		pA
IB	input bias current (see Note 4)	VIC = 1 V	85°C		175	2000		200	2000	pr
	Common-mode input		25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		v
VICR	voltage range (see Note 5)	perature, V _{DD} =	Full range	-0.2 to 1.8			-0.2 to 3.8	PARAS		V
	5°C 0.03	V _{IC} = 1 V,	25°C	1.75	1.9		3.2	3.8		
Vон	High-level output voltage	V _{ID} = 100 mV, I _{OH} = -1 mA	Full range	1.7			3	nu la els	Slaw	V
	\$0.0 D*8	$V_{IC} = 1 V,$	25°C		115	150		95	150	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	f and		190	esionti	adinsis	190	mV
	Large-signal differential	$V_{IC} = 1 V,$	25°C	50	400		50	520		
AVD	voltage amplification	R _L = 1 MΩ, See Note 6	Full range	50	(d)	Supplies .	50	glup mur	nixeM.	V/m\
	88 0%8	V _O = 1 V,	25°C	65	88		65	94	Unit	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR} min,$ $R_S = 50 \Omega$	Full range	60			60			dB
(0) (D	Supply-voltage rejection ratio	$V_{IC} = 1 V, V_{O} = 1 V,$	25°C	70	86		70	86	autor -	dP
KSVR	(AVDD/AVIO)	Rs = 50 Ω	Full range	65			65			dB
	Supply surrent	V _O = 1 V, V _{IC} = 1 V,	25°C		24	68		39	68	
DD	Supply current	No load	Full range			108			108	μA

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O(PP) = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



operating characteristics at specified free-air temperature, V_{DD} = 3 V

	BARANETER STATE	TEAT		ТА	TLV2324I	
	PARAMETER	TEST C	TEST CONDITIONS		MIN TYP MAX	UNIT
0.0	XAM GYT MM XAM GYT	$V_{IC} = 1 V,$	$V_{I(PP)} = 1 V,$	25°C	0.02	
SR	Slew rate at unity gain	$R_L = 1 M\Omega$, See Figure 30	CL = 20 pF,	85°C	0.02	V/µs
vn	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	68	nV√/Hz
Derry	Maximum output swing bandwidth	Vo = VoH,	CL = 20 pF,	25°C	2.5	kHz
BOM	Maximum output swing bandwidth	$R_L = 1 M\Omega$,	See Figure 30	85°C	againer led 2 hours to	KHZ
D.	Unity-gain bandwidth	V _I = 10 mV,	CL = 20 pF,	25°C	27	kHz
B ₁	Onity-gain bandwidth	$R_L = 1 M\Omega$,	See Figure 32	85°C	21	KHZ
	8.0	$V_{I} = 10 \text{ mV},$	f = B ₁ ,	-40°C	39°	
φm	Phase margin	C _L = 20 pF,	R _L = 1 MΩ,	25°C	34°	
		See Figure 32		85°C	28°	1

operating characteristics at specified free-air temperature, V_{DD} = 5 V

V	PARAMETER TEST CONDITIONS		ONDITIONS	T.	TLV2324I	LINUT	
	PARAMETER	TESTO	UNDITIONS	TA	MIN TYP MAX	UNIT	
	5.8 5.6 8.7	$V_{IC} = 1 V$,	Numer 1V	25°C	0.03		
SR	Slew rate at unity gain	$R_L = 1 M\Omega$,	VI(PP)= 1 V	85°C	0.03	HOV	
SR	and the second se	CL = 20 pF,	N 05W	25°C	0.03	V/µs	
	16 160 160	See Figure 30	VI(PP) = 2.5 V	85°C	0.02	1	
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	68	nV/√Hz	
Vent	Man for an ender dan der berecht dub	Vo = VoH,	$C_1 = 20 \text{pF},$	25°C	5		
BOM	Maximum output swing bandwidth	$R_L = 1 M\Omega$,	See Figure 30	85°C	4	kHz	
D.	Unity-gain bandwidth	V _I = 10 mV,	CL = 20 pF,	25°C	85	1.1.1-	
B ₁	Unity-gain bandwidth	$R_L = 1 M\Omega$,	See Figure 32	85°C	55	kHz	
		V _I = 10 mV,	f = B ₁ ,	-40°C	38°		
φm	Phase margin	CL = 20 pF,	$R_L = 1 M\Omega$,	25°C	34°	RVal	
		See Figure 32		85°C	28°	110	

Bupply ourrant



-					TLV2324Y					
	PARAMETER	TEST CONDITIONS		V _{DD} = 3 V			V _{DD} = 5 V			UNIT
			a series and the second se	MIN TYP		MAX	MIN	TYP	MAX	
VIO	Input offset voltage	$V_{O} = 1 V,$ R _S = 50 Ω ,	$V_{IC} = 1 V,$ $R_L = 1 M\Omega$		1.1	10	feallo lu	1.1	10	mV
10	Input offset current (see Note 4)	V _O = 1 V,	V _{IC} = 1 V		0.1			0.1	Million -	pА
IIB	Input bias current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.6	and the state	balakt	0.6	and I	pА
VICR	Common-mode input voltage range (see Note 5)	mparatore missio mode Inper	and the second second second second	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2	and to a second second	v
VOH	High-level output voltage	$V_{IC} = 1 V,$ $I_{OH} = -1 mA$	V _{ID} = 100 mV,	1.75	1.9	loy logh	3.2	3.8	JoV	V
VOL	Low-level output voltage	$V_{IC} = 1 V,$ $I_{OL} = 1 mA$	V _{ID} = 100 mV,		115	150		95	150	mV
AVD	Large-signal differential voltage amplification	V _{IC} = 1 V, (see Note 6)	R _L = 1 MΩ,	50	400		50	520	Copyra Inconstruction	V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V,$ R _S = 50 Ω	$V_{IC} = V_{ICR}min$,	65	88	ugni abs	65	94	DIV.	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{O} = 1 V,$ R _S = 50 Ω	V _{IC} = 1 V,	70	86	ha	70	86	adi	dB
IDD	Supply current	V _O = 1 V, No load	V _{IC} = 1 V,		24	68	etes v	39	68	μА

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

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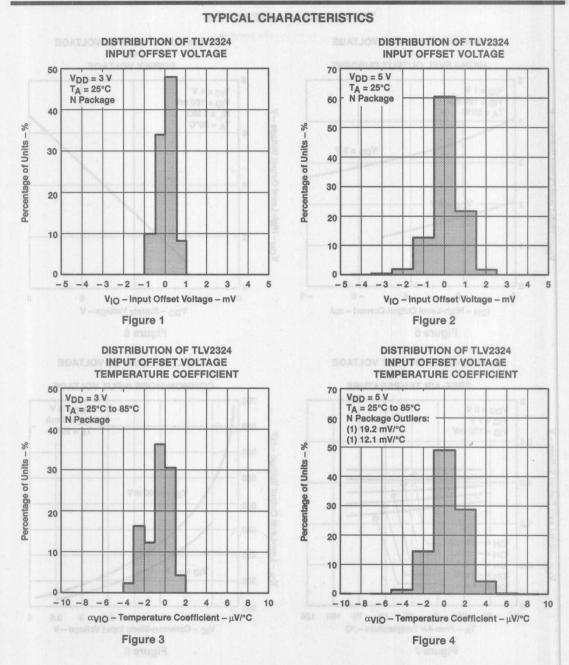
	Table of	Graphs	
AM TAY	T NUM XAM TYP NUM		FIGURE
VIO	Input offset voltage	Distribution	1,2
ανιο	Input offset voltage temperature coefficient	Distribution	3, 4
-		vs Output current	5
Vон	High-level output voltage	vs Supply voltage	6
8.0		vs Temperature	/ tue oi ebon 7 nomine D
0.1	- 2 23 4 4	vs Common-mode input voltage	8
	Low-level output voltage	vs Temperature	9, 11
VOL	Low-level output voltage	vs Differential input voltage	10
		vs Low-level output current	12
A		vs Supply voltage	13
AVD	Large-signal differential voltage amplification	vs Temperature	14
IB/IO	Input bias and offset currents	vs Temperature	15
VIC	Common-mode input voltage	vs Supply voltage	16
	Supply current	vs Supply voltage	17
DD	Supply current	vs Temperature	18
SR	Slew rate	vs Supply voltage	19
90	Siew rate	vs Temperature	20
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	21
	Unity-gain bandwidth	vs Temperature	22
B ₁	Unity-gain bandwidth	vs Supply voltage	23
AVD	Large-signal differential voltage amplification	vs Frequency	24, 25
		vs Supply voltage	26
¢m	Phase margin	vs Temperature	27
		vs Load capacitance	28
Vn	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS



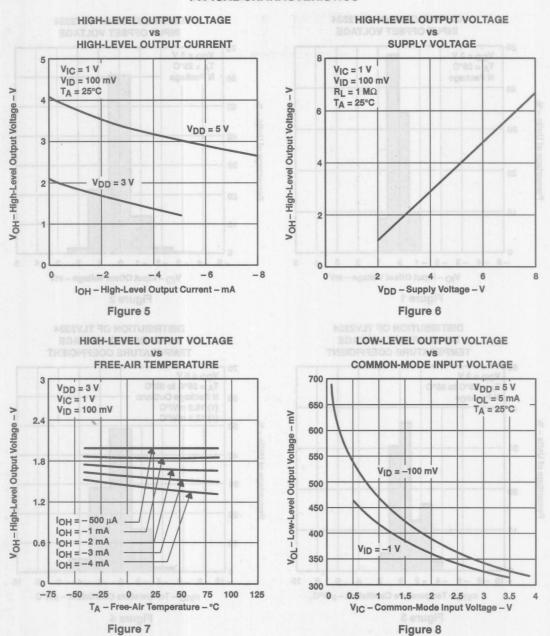
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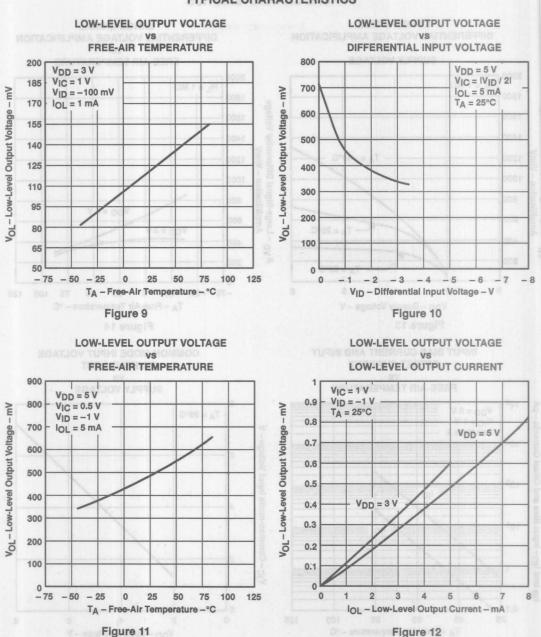
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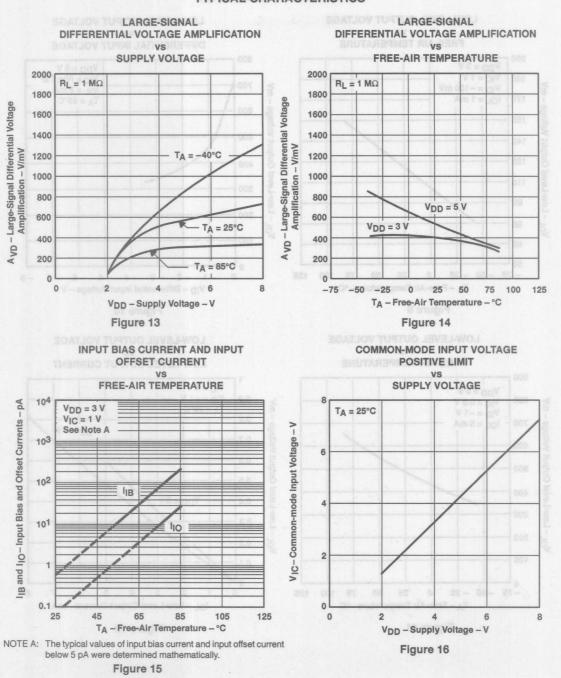
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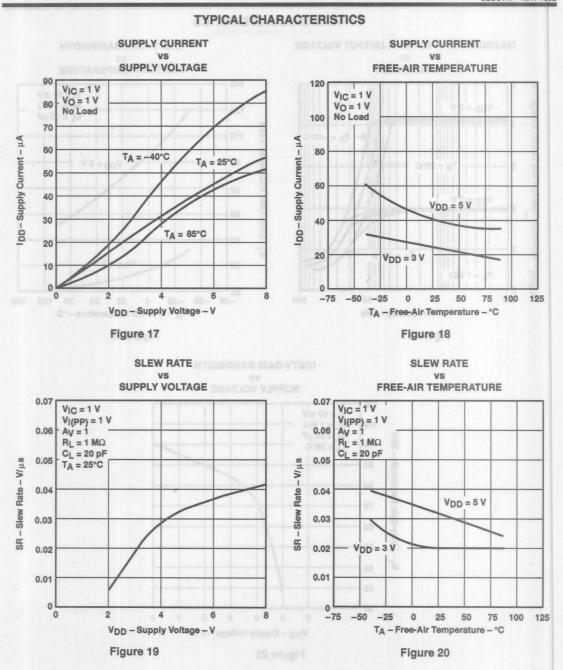


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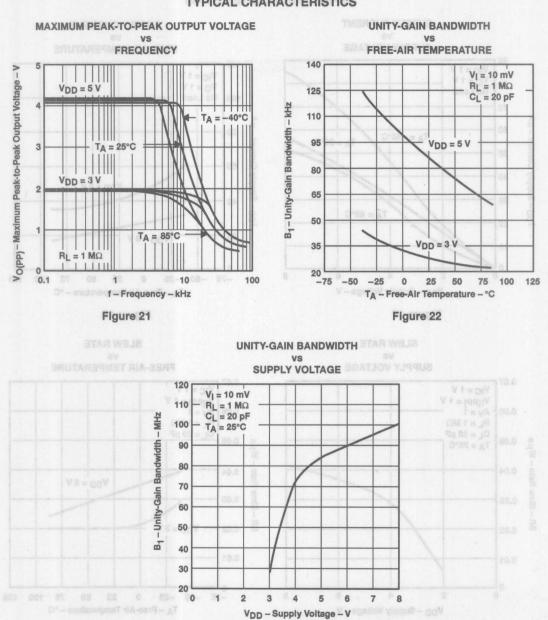


LINCMOS™ LOW-VOLTAGE LOW-POWER QUAD OPERATIONAL AMPLIFIERS SLOS111 - MAY 1992





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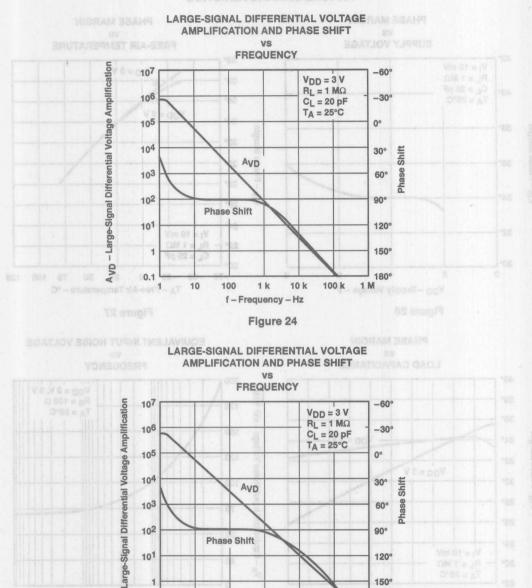
TYPICAL CHARACTERISTICS



Figure 23

TLV2324I, TLV2324Y LinCMOS™ LOW-VOLTAGE LOW-POWER QUAD OPERATIONAL AMPLIFIERS SLOS111 - MAY 1992

TYPICAL CHARACTERISTICS



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FXAS

1 k

f - Frequency - Hz Figure 25

10 k

120° 150°

100 k 1 M

180°

101

1

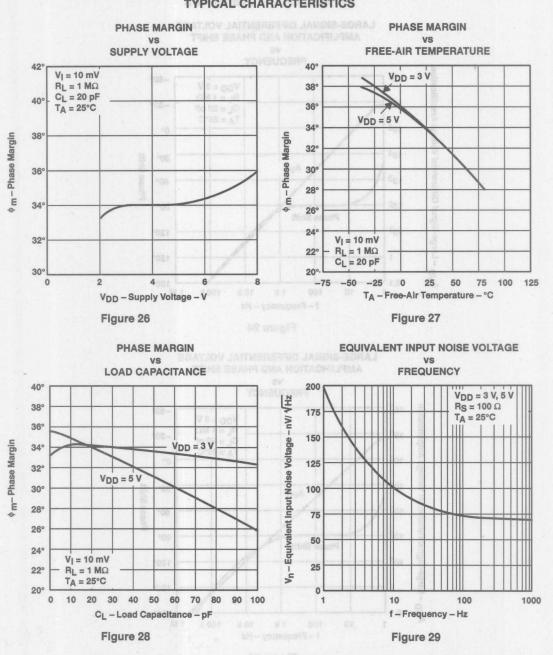
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10

100

AVD-I 0.1

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TYPICAL CHARACTERISTICS



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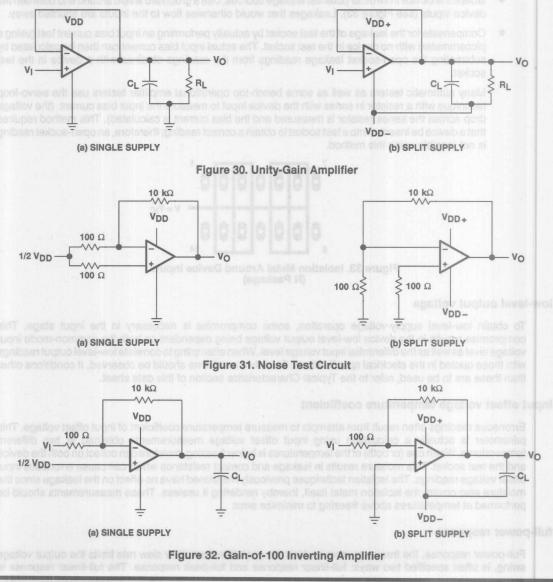
LINCMOS™ LOW-VOLTAGE LOW-POWER QUAD OPERATIONAL AMPLIFIERS SLOS111 - MAY 1992

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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2324 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



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TLV2324I, TLV2324Y LinCMOSTM LOW-VOLTAGE LOW-POWER QUAD OPERATIONAL AMPLIFIERS SLOS111 - MAY 1992

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2324 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

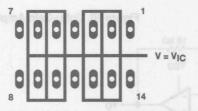


Figure 33. Isolation Metal Around Device Inputs (N Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

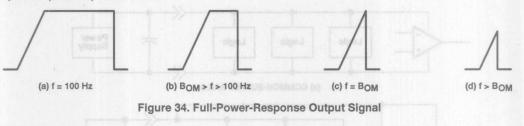


TLV2324I, TLV2324Y LinCMOS™ LOW-VOLTAGE LOW-POWER QUAD OPERATIONAL AMPLIFIERS

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2324 performs well using dualpower supplies (also called balanced or split supplies), the design is optimized for singlesupply operation. This includes an input commonmode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

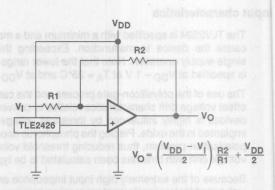


Figure 35. Inverting Amplifier With Voltage Reference

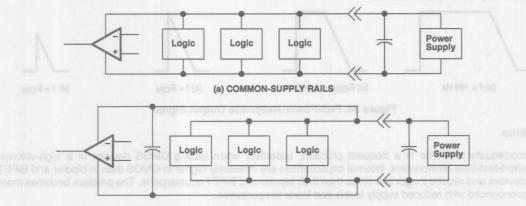


TLV2324I, TLV2324Y LinCMOSTM LOW-VOLTAGE LOW-POWER QUAD OPERATIONAL AMPLIFIERS

APPLICATION INFORMATION

single-supply operation (continued)

- The TLV2324 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:
 - Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
 - Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive
 decoupling is often adequate; however, RC decoupling may be necessary in high-frequency
 applications.



(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)



input characteristics

The TLV2324 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2324 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

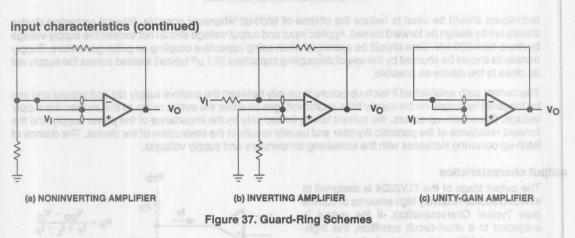
Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2324 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



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APPLICATION INFORMATION



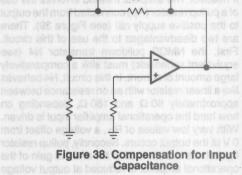
noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2324 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

electrostatic-discharge protection



The TLV2324 incorporates an internal electrostatic-discharge (ESD)-protection circuit that

prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2324 inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up; however,



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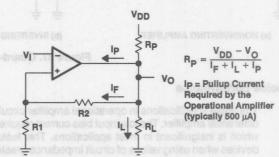
techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rail as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with the increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2324 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this highcurrent capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2324 possesses excellent high-level output voltage and current capability. methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60Ω and 180Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.





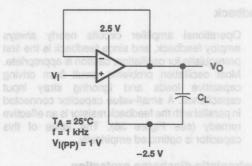


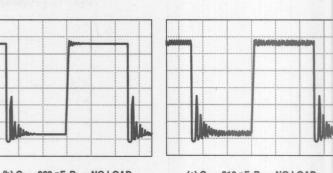
Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2324 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

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APPLICATION INFORMATION





output characteristics (continued)

(b) $C_L = 260 \text{ pF}$, $R_L = \text{NO LOAD}$

(c) $C_L = 310 \text{ pF}$, $R_L = \text{NO LOAD}$

Figure 41. Effect of Capacitive Loads



TLV23241, TLV23241, TLV23241, TLV23241, Incmost Low-Poltage Low-Power QUAD OPERATIONAL AMPLIFERS

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	1.1		

(a) QL = 310 pR, RL = NO LOAE

GAOJ ON = 39, 30 002 = 30 (03)

(a) OL = 20 př. RL = NO LOA

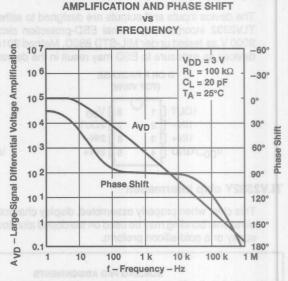
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LARGE-SIGNAL DIFFERENTIAL VOLTAGE

- Wide Range of Supply Voltages Over **Specified Temperature Range:** $T_{\Delta} = -40^{\circ}C$ to 85°C . . . 2 V to 8 V
 - Fully Characterized at 3 V and 5 V
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range** . Extends Below the Negative Rail and up to V_{DD} -1 V at T_A = 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10¹² Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

description

The TLV2332 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike the TLV2322 which is optimized for ultra-low power, the TLV2332 is



designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only 310 µA per amplifier over full temperature range, the TVL2332 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifier's typical slew rate is 0.38 V/µs and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels. The TLV2332 operational amplifiers are especially well suited for use in low-current or battery-powered applications.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOSTM technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV2332 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline package (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

46-0 10 20(2)	TOBA	PACKAGED DEVICES				
TA	A VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)	
-40°C to 85°C	9 mV	TLV2332ID	TLV2332IP	TLV2332IPWLE	TLV2332Y	

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2332IDR). The PW package is only available left-end taped and reeled (e.g., TLV2332IPWLE).

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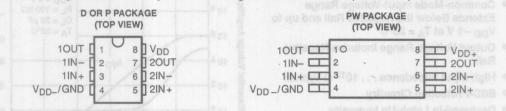
PRODUCTION DATA Information is current as of publication data. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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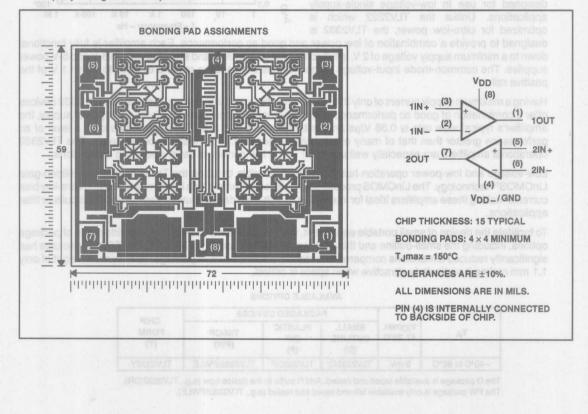
description (continued)

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2332 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



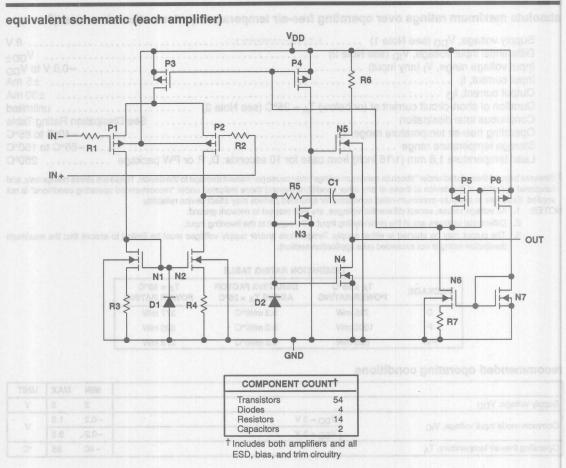
TLV2332Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2332I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



JMENTS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) 8 V Differential input voltage, V_{ID} (see Note 2) V_{DD} Input voltage range, V_I (any input) -0.3 V to V_{DD} Input current, I_I ± 5 mA Output current, I_O ± 30 mA Duration of short-circuit current at (or below) $T_A = 25^{\circ}$ C (see Note 3) unlimited Continuous total dissipation See Dissipation Rating Table	± CAAde
Operating free-air temperature range, T _A 40°C to 85°C	С
Storage temperature range -65°C to 150°C Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package 260°C	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

	DISSIPATION RATING TABLE					
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING			
D	725 mW	5.8 mW/°C	377 mW			
P	1000 mW	8.0 mW/°C	520 mW			
PW	525 mW	4.2 mW/°C	273 mW			

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, VDD	AC EXCERTS I	2	8	V
Common mode insutualtage Via	V _{DD} = 3 V	-0.2	1.8	V
Common-mode input voltage, VIC	V _{DD} = 5 V	-0.2	3.8	V
Operating free-air temperature, TA	te one exemples mot excurse *	-40	85	°C



		in the second second		TLV2332I						
	PARAMETER	TEST CONDITIONS	TAT	V	DD = 3 1	1	V _{DD} = 5 V			UNIT
		Vinigan's	Via	MIN	TYP	MAX	MIN	TYP	MAX	
Vio	Input offset voltage	$V_{O} = 1 V,$ $V_{IC} = 1 V,$	25°C	997 - 199	0.6	9	ning gala	1.1	9	mV
vi0	input onset voltage	R _S = 50 Ω, R _L = 100 kΩ	Full range	Beel .		11	ealon tu	gril traja	11	niv o
αΛΙΟ	Average temperature coefficient of input offset voltage	C), = 20 pF. Bas Figura 30	25°C to 85°C	OV M	1	hwbriad.	golwa: luc	1.7	dista.	μV/°C
he	Input offset current (see Note 4)	V _O = 1 V,	25°C	- 12	0.1			0.1		-
IIO	input onset current (see Note 4)	VIC = 1 V	85°C	e fil	22	1000	1 DOIDHEN	24	1000	pА
IIB	Input bias current (see Note 4)	V _O = 1 V,	25°C		0.6			0.6		pА
IB	mput bias current (See Note 4)	VIC = 1 V	85°C	0	175	2000		200	2000	pA
			St oug?	-0.2	-0.3		-0.2	-0.3		
	Common-mode input		25°C	to 2	to 2.3		to 4	to 4.2		V
VICR	voltage range (see Note 5)	oerature, V _{DD} e l	1310 100-0	-0.2	Bar or ca	0.200 00	-0.2	100101	10 1971	icity of
TIMU	TAN TY NOS	exoma	Full range	to 1.8			to 3.8			V
	5°C 1 0.48	$V_{IC} = 1 V,$	25°C	1.75	1.9		3.2	3.9		
VOH	High-level output voltage	V _{ID} = 100 mV, I _{OH} = -1 mA	Full range	1.7			3	to be the	Stew	V
	55.0°	VIC = 1 V,	25°C	1900	115	150		95	150	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	Te 1	-181411-18	190	ention tu	ant their	190	mV
	Large-signal differential	VIC = 1 V,	25°C	25	83		25	170		
AVD	voltage amplification	R _L = 100 kΩ, See Note 6	Full range	15	181	iwbridd	15	ano neg	ristani.	V/mV
OMDD		$V_{O} = 1 V,$	25°C	65	92		65	91	winds ?	-10
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, R _S = 50 Ω	Full range	60			60			dB
ksvr	Supply-voltage rejection ratio	$V_{IC} = 1 V, V_{O} = 1 V,$	25°C	70	94		70	94	Pitera	dB
SVR	(ΔV _{DD} /ΔV _{IO})	R _S = 50 Ω	Full range	65			65			aB
	Supply ourrept	$V_{O} = 1 V, V_{IC} = 1 V,$	25°C		160	500		210	560	
DD	Supply current	No load	Full range			620		-	800	μA

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



		TEOTO	TEST CONDITIONS		TLV2332		
	PARAMETER	TEST G			MIN TYP	MAX	UNIT
	TYP MAX MIN TYP MAX	$V_{IC} = 1 V,$	$V_{I(PP)} = 1 V,$	25°C	0.38		
SR	Slew rate at unity gain	$R_L = 100 k\Omega$, See Figure 30	CL = 20 pF,	85°C	0.29		V/µs
v _n	Equivalent input noise voltage	f =1 kHz, See Figure 31	R _S = 100 Ω,	25°C	32		nV/√Hz
0		Vo = Voh,	C1 = 20 pF,	25°C	34	Avorage	Lille
BOM	Maximum output swing bandwidth	R _L = 100 kΩ,	See Figure 30	85°C	32	Judai te	kHz
-		$V_{I} = 10 \text{ mV},$	C1 = 20 pF,	25°C	300	to Bloot	kHz
B ₁	Unity-gain bandwidth	R _L = 100 kΩ,	See Figure 32	85°C	235		KHZ
·	0.6	$V_{I} = 10 \text{ mV},$	f = B1.	-40°C	42°	let warned	- mil
φm	Phase margin	CL = 20 pF,	R _L = 100 kΩ,	25°C	39°		
		See Figure 32		85°C	36°		1

operating characteristics at specified free-air temperature, V_{DD} = 3 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V

V.	PARAMETER	TEOTO	TEST CONDITIONS		TLV23321		
		TEST C	JNDITIONS	TA	MIN TYP MAX	UNIT	
	1.9	$V_{IC} = 1 V_{i}$	V	25°C	0.43		
SR	Class sata at units ania	$R_L = 100 \text{ k}\Omega,$	VI(PP) = 1 V	85°C	0.35	N/Los	
SR	Slew rate at unity gain	CL = 20 pF,	New OFN	25°C	0.40	V/µs	
		See Figure 30	VI(PP) = 2.5 V	85°C	0.32	in the	
vn	Equivalent input noise voltage	f =1 kHz, See Figure 31	R _S = 100 Ω,	25°C	32	nV/√H	
-	Mandaman and and an day barrah dabb	Vo = VoH,	CL = 20 pF,	25°C	55	1.11	
BOM	Maximum output swing bandwidth	R _L = 100 kΩ,	See Figure 30	85°C	45	kHz	
		V _I = 10 mV,	Ci = 20 pF,	25°C	525	Let Im	
B ₁	Unity-gain bandwidth	R _L = 100 kΩ,	See Figure 32	85°C	370	kHz	
	And the second sec	$V_{I} = 10 \text{ mV},$	f = B ₁ ,	-40°C	43°		
φm	Phase margin	C _L = 20 pF,	R _L = 100 kΩ,	25°C	40°	101/90	
		See Figure 32		85°C	38°		

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The typical values of input blan operant and input official operant below 6 pA are determined methodiate.
 This range also applies to each input lectividually.





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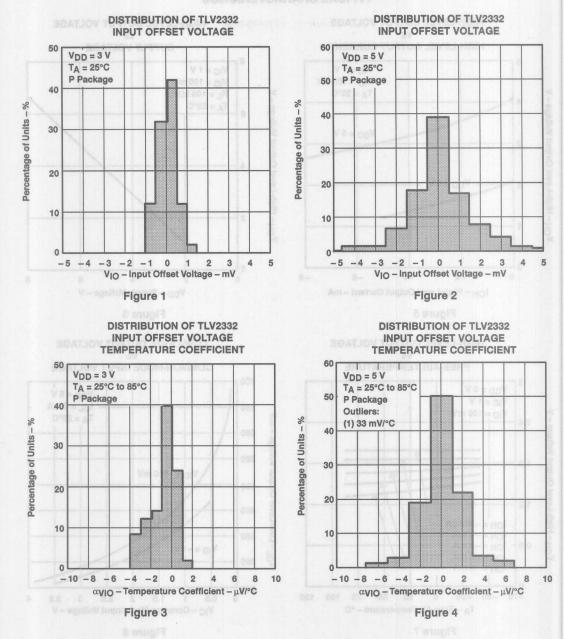
				TLV2332Y						
PARAMETER		TEST CONDITIONS		V	DD = 3	V	V _{DD} = 5 V			UNIT
				MIN	MIN TYP I		MIN TYP		MAX	
VIO	Input offset voltage	$V_{O} = 1 V,$ R _S = 50 Ω ,	VIC = 1 V, RL = 100 kΩ		0.6	9	issila nu	1.1	9	mV
10	Input offset current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.1		A STATISTICS	0.1	AV-	pA
IIB	Input bias current (see Note 4)	V _O = 1 V,	VIC = 1 V	- (0.6			0.6		pА
	Common mode input voltage	light voluege	19 24	-0.2	-0.3	the should be	-0.2	-0.3	HOY	
VICR	Common-mode input voltage range (see Note 5)	i indisnegri	oT av	to	to		to	to		V
	Tange (see Note 5)	oni nisam-norm	sO av	2	2.3		4	4.2		
VOH	High-level output voltage	$V_{IC} = 1 V,$ $I_{OH} = -1 mA$	V _{ID} = 100 mV,	1.75	1.9	Nov Juch	3.2	3.9	Vol	V
VOL	Low-level output voltage	$V_{IC} = 1 V,$ $I_{OL} = 1 mA$	V _{ID} = 100 mV,		115	150		95	150	mV
AVD	Large-signal differential voltage amplification	VIC = 1 V, See Note 6	RL = 100 kΩ,	25	83	nerellio i	25	170	ava	V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V,$ R _S = 50 Ω	$V_{IC} = V_{ICR} min,$	65	92	ndar epe	65	91		dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{O} = 1 V,$ $R_{S} = 50 \Omega$	V _{IC} = 1 V,	70	94	in	70	94	ant	dB
IDD	Supply current	$V_{O} = 1 V,$ No load	V _{IC} = 1 V,		160	500	edan ya	210	560	μА

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

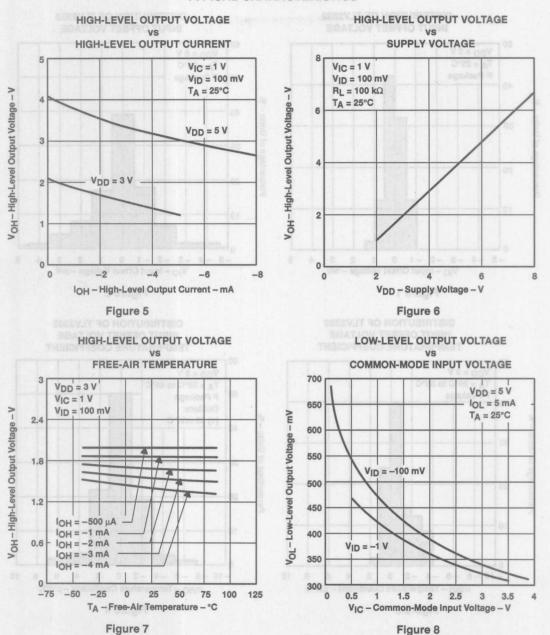


W dA	ANNA XANG NYT WINA		FIGURE
VIO	Input offset voltage	Distribution	1,2
ανιο	Input offset voltage temperature coefficient	Distribution	3, 4
	and the second	vs Output current	5
VOH	High-level output voltage	vs Supply voltage	6
		vs Temperature	7
4.2	* 6.S S	vs Common-mode input voltage	8
	Low-level output voltage	vs Temperature	9, 11
VOL	Low-level output voltage	vs Differential input voltage	10
		vs Low-level output current	12
	I I I PR I I I I I I I I I I I I I I I I	vs Supply voltage	13
AVD	Large-signal differential voltage amplification	vs Temperature	14
IB/IO	Input bias and offset currents	vs Temperature	15
VIC	Common-mode input voltage	vs Supply voltage	16
	Construction	vs Supply voltage	17
DD	Supply current	vs Temperature	18
SR	Slew rate	vs Supply voltage	19
SR	Slew rate	vs Temperature	20
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	21
D.	Unity only handwidth	vs Temperature	22
B ₁	Unity-gain bandwidth	vs Supply voltage	23
AVD	Large-signal differential voltage amplification and phase shift	vs Frequency	24, 25
		vs Supply voltage	26
φm	Phase margin	vs Temperature	27
		vs Load capacitance	28
Vn	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24.25

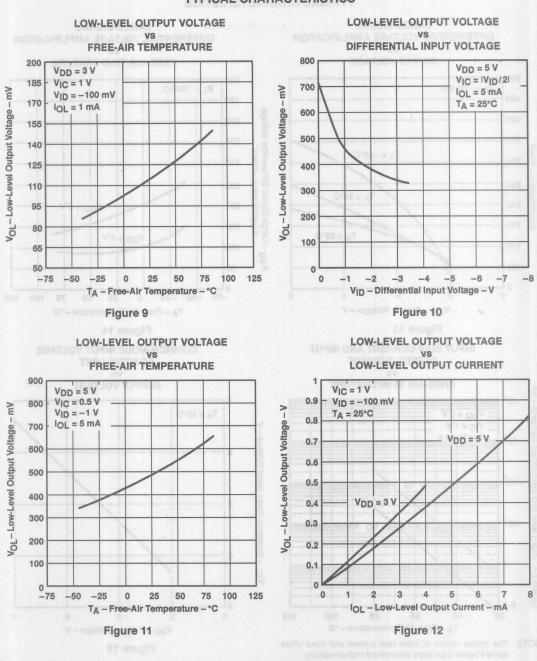






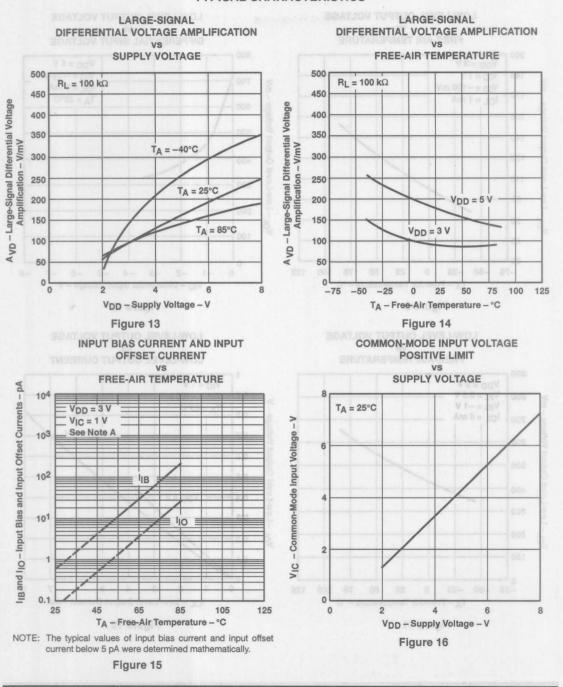






INSTRUMENTS

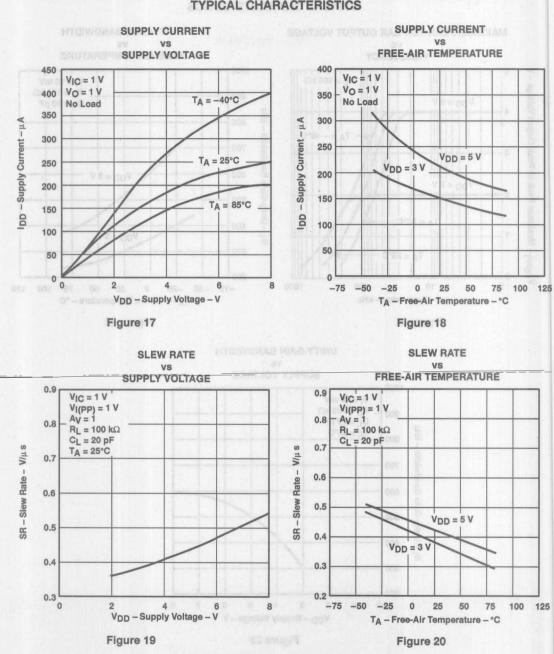
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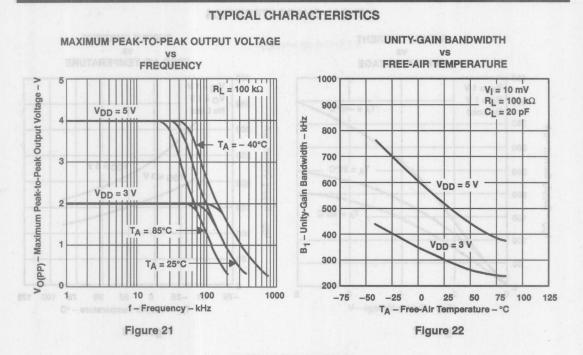
TYPICAL CHARACTERISTICS

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SLOS112 - MAY 1992







UNITY-GAIN BANDWIDTH VS SUPPLY VOLTAGE 1000 $V_I = 10 \text{ mV}$ $R_L = 100 k\Omega$ 900 CL = 20 pF - KHz TA = 25°C 800 Bandwidth 700 600 - Unity-Gain 500 400 ň 300 200 0 1 2 3 4 5 6 7 8 VDD - Supply Voltage - V Figure 23



2-124

TYPICAL CHARACTERISTICS

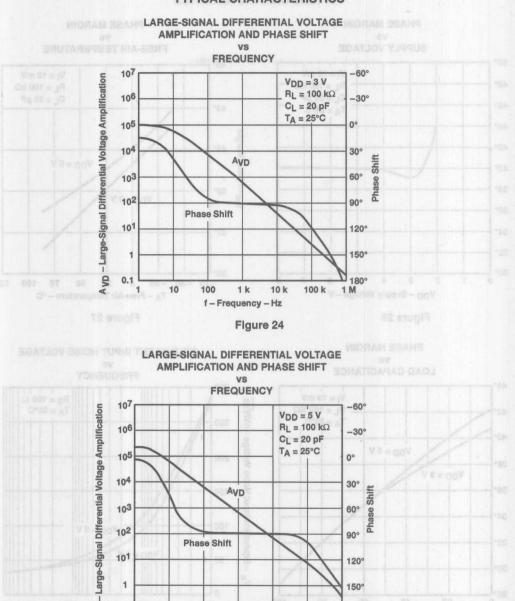


Figure 25

10 k

100 k

1 k

f - Frequency - Hz

A VD 0.1

1

10

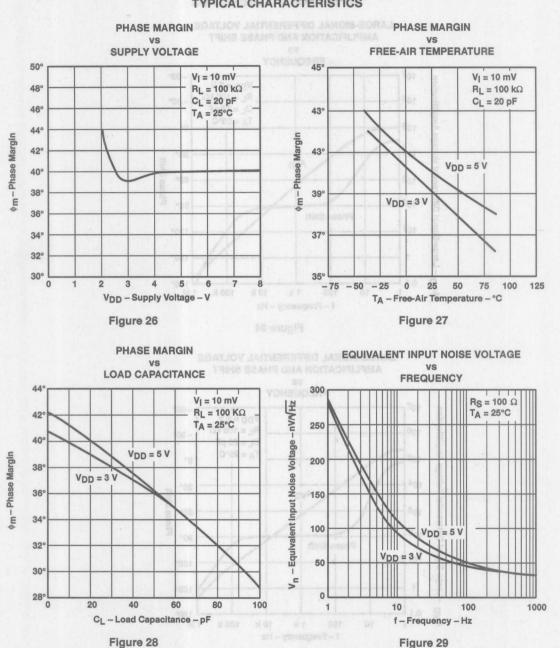
100

150°

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1 M





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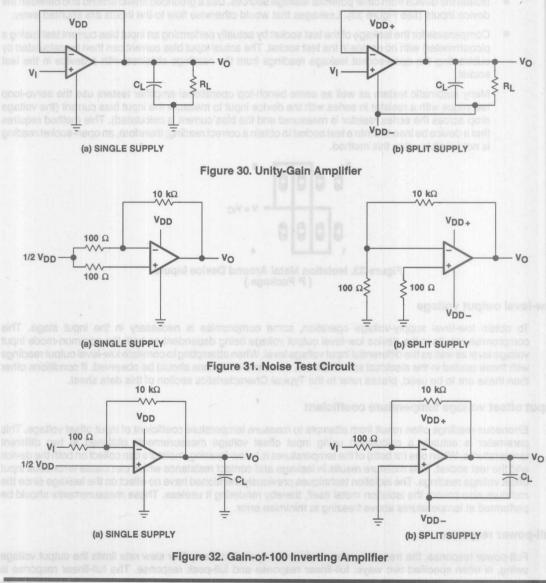
TYPICAL CHARACTERISTICS

2-126

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2332 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.





PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2332 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a
 picoammeter) with no device in the test socket. The actual input bias current can then be calculated by
 subtracting the open-socket leakage readings from the readings obtained with a device in the test
 socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

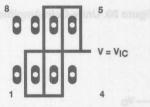


Figure 33. Isolation Metal Around Device Inputs (P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is



PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

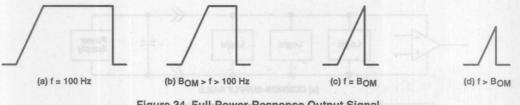


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2332 performs well using dualpower supplies (also called balanced or split supplies), the design is optimized for singlesupply operation. This includes an input commonmode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to VDD/2, while consuming very little power and is suitable for supply voltages of greater than 4 V.

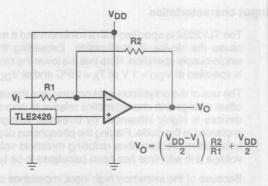


Figure 35. Inverting Amplifier With Voltage Reference

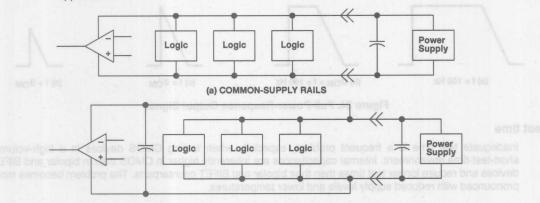


APPLICATION INFORMATION

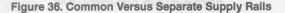
single-supply operation (continued)

The TLV2332 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive
 decoupling is often adequate; however, RC decoupling may be necessary in high-frequency
 applications.



(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)



input characteristics

The TLV2332 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

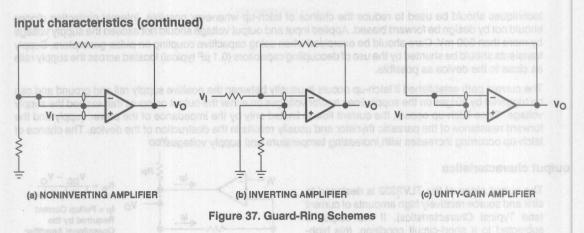
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2332 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2332 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



APPLICATION INFORMATION



noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2332 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifiers circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

electrostatic-discharge protection

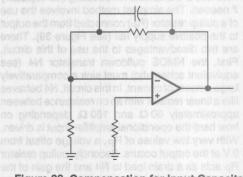


Figure 38. Compensation for Input Capacitance

The TLV2332 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to

2000 V as tested under MIL-STD-883C. Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2332 inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up; however,



APPLICATION INFORMATION

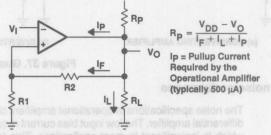
techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2332 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this highcurrent capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2332 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60Ω and 180Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.





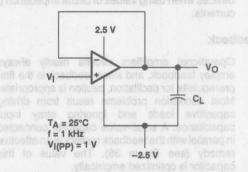


Figure 40. Test Circuit for Output Characteristics

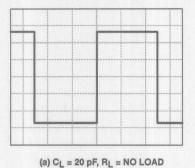
All operating characteristics of the TLV2332 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

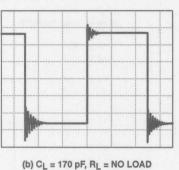
Nocause CMOS devices are susceptible to later-up due to their inheren parasitic thyristore, the TLV8332 input

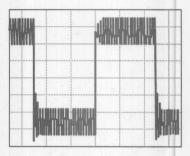


APPLICATION INFORMATION









(c) CL = 190 pF, RL = NO LOAD

Figure 41. Effect of Capacitive Loads



TLV23321, TLV23321, TLV23321, LincMOSTM LOW-VOLTAGE MEDIUM-POWER DUAL OPERATIONAL AMPLIFIERS

APPLICATION IMPORMATION

outout characteristics (continued)



AND - ADDA DA - MOLANA

(a) OL = 20 pK RL = 100 LOAL

control And Control of the Strephy of the Strephy

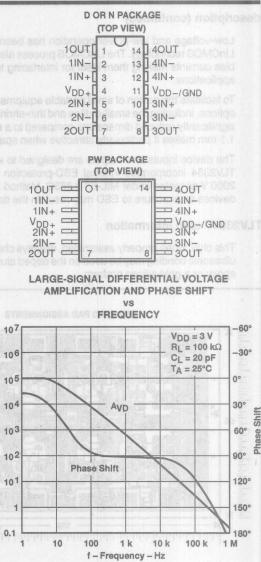
- Wide Range of Supply Voltages Over Specified Temperature Range:
 T_Δ = -40°C to 85°C...2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10¹² Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

description

The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike the TLV2324 which is optimized for ultra-low power, the TLV2334 is designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of -40° C to 85° C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only $300 \ \mu A$ per amplifier over full temperature range, the TLV2334 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifier's typical slew rate is 0.38 V/µs and its bandwidth is $300 \ \text{kHz}$. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels.

The TLV2334 operational amplifiers are especially well suited for use in low current or battery-powered applications.



AVAILABLE OPTIONS

Amplification

Voltage

Differential

2

-Sign

Large

S

4

ſ	3.66	in summing	P	ACKAGED DE	VICES	01110
		V _{IO} max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	CHIP FORM (Y)
ľ	-40°C to 85°C	10 mV	TLV2334ID	TLV2334IN	TLV2334IPWLE	TLV2334Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2334IDR). The PW package is only available left-end taped and reeled (e.g., TLV2334IPWLE).

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description (continued)

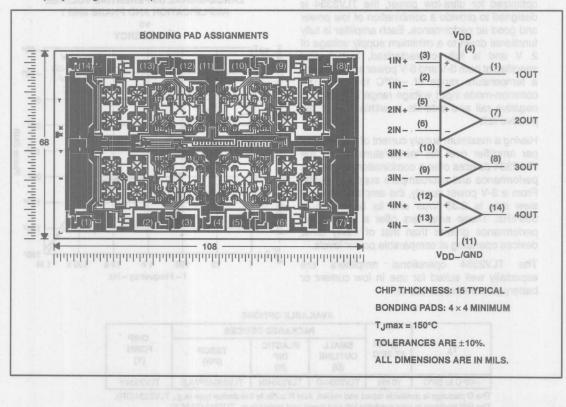
Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV2334 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

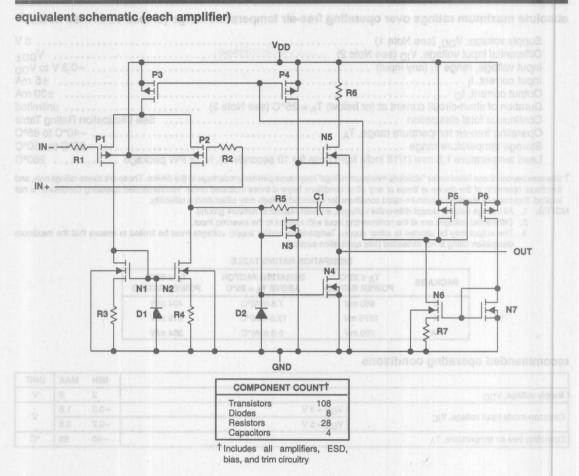
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2334 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2334Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2334I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VDD. (see Note 1)	8 V
Differential input voltage, VID (see Note 2)	
Input voltage, range VI (any input)	
Input current, I ₁	±5 mA
Output current, Io	±30 mA
Duration of short-circuit current at (or below) T _A = 25 °C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, TA	40°C to 85°C
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
D	950 mV	7.6 mW/°C	494 mW
N	1575 mV	12.6 mW/°C	819 mW
PW	700 mV	5.6 mW/°C	364 mW

recommended operating conditions

	Provide and a second provide and a second second	MIN	MAX	UNIT
Supply voltage, VDD	A CONTRACT OF A	2	8	V
	V _{DD} = 3 V	-0.2	1.8	N
Common-mode input voltage, VIC	$V_{DD} = 5 V$	-0.2	3.8	V
Operating free-air temperature, TA	and the second s	-40	85	°C



	BADGEVIT · TEVERAB			TLV2334I							
	PARAMETER	TEST CONDITIONS	TAT	V	DD = 3 \	1	V _{DD} = 5 V			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
VIO	Input offset voltage $V_O = 1 V$, $V_{IC} = 1 V$, $R_S = 50 \Omega$,		25°C	HL =	0.6	10	nuap VII	1.1	10	mV	
×10	input onset voltage	$R_{L} = 100 \text{ k}\Omega$	Full range			12		invitaet	12		
αΛΙΟ	Average temperature coefficient of input offset voltage		25°C to 85°C	508 • OV	1			1.7		μV/°C	
	Innut offect ourrent (and Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	- RI	0.1			0.1		pA	
10	Input offset current (see Note 4)	vO = 1 v, $v C = 1$ v	85°C	miV	22	1000	Harris	24	1000	рА	
lun	Input bias current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	n JA	0.6			0.6		pA	
IB	input bias current (See Note 4)	v0=+v, v10=+v	85°C	w.N	175	2000		200	2000	pr	
VICR Common-mode input voltage range (see Note 5)	Pir = 100 Hits	25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2	Phase	V		
	ersture, V _{DD} = 1	Full range	-0.2 to 1.8	nloso	e is c	-0.2 to 3.8	arectu	ng ch	V		
	XAM GYT MM	V _{IC} = 1 V,	25°C	1.75	1.9		3.2	3.9			
VOH	High-level output voltage	V _{ID} = 100 mV, I _{OH} = -1 mA	Full range	1.7			3			V	
Ruhv	5°O 0.40	$V_{IC} = 1 V,$	25°C		115	150	mag ya	95	150		
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	1.100	andra za tana ta	190			190	mV	
BRyvVn	Large-signal differential	VIC = 1 V,	25°C	25	83	apolio	25	170	Equava		
AVD	voltage amplification	RL = 100 kΩ, See Note 6	Full range	15	cit	hickores	15	istus mu	-	V/mV	
	PO 45	V _O = 1 V,	25°C	65	92		65	91			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min,$ Rs = 50 Ω		Full range	60			60	anad qiar	Unity	dB
kours	Supply-voltage rejection ratio	$V_{DD} = 3 V \text{ to } 5 V,$	25°C	70	94		70	94		dB	
ksvr	VIC = 1 V, VO = 1 V, F	Full range	65			65	margin	Phased	aB		
Inc	Supply auropt	$V_{O} = 1 V, V_{IC} = 1 V,$	25°C	and and and	320	1000		420	1120		
IDD	Supply current	No load	Full range			1200			1600	μA	

[†] Full range is -40°C to 85°C. NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.

5. This range also applies to each input individually. 6. At $V_{DD} = 5 V$, $V_O = 0.25 V$ to 2 V; at $V_{DD} = 3 V$, $V_O = 0.5 V$ to 1.5 V.



	TEVERSVIT	TEST CONDITIONS		TA	TLV2334I		LIAUT	
	PARAMETER	TEST CC	TEST CONDITIONS		MIN TYP	YP MAX	UNIT	
0.0	TYP MAX MIN TYP MAX	w rate at unity gain $ \begin{array}{ll} V_{IC} = 1 \ V, & V_{I(PP)} = 1 \ V, \\ R_L = 100 \ k\Omega, & C_L = 20 \ pF, \\ See \ Figure \ 30 \end{array} $		25°C	0.	38		
SR	Siew rate at unity gain		CL = 20 pr,	85°C	0.	29	V/µs	
v _n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	co stateloor	32	nV/√Hz	
- Contract		Vo = VoH,	CL = 20 pF,	25°C	egetlov te	34	kHz	
BOM	Maximum output swing bandwidth	$R_L = 100 k\Omega$,	See Figure 30	85°C		32		
	10001 AS	V ₁ = 10 mV,	$C_1 = 20 \text{pF},$	25°C	3	00		
B ₁	Unity-gain bandwidth	R _L = 100 kΩ,	See Figure 32	85°C	2	35	kHz	
1994	175 2000 2000	V ₁ = 10 mV, f = B ₁	VI = 10 mV f = Bt	f = B ₁ ,	-40°C	4	2°	
φm	Phase margin	and the second	R _L = 100 kΩ,	25°C	3	19°	1	
				85°C	3	6°	1	

operating characteristics at specified free-air temperature, V_{DD} = 3 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEOT	TEST CONDITIONS		TLV2334I	LINUT
		TEST CONDITIONS		TA	MIN TYP MAX	
V	and the second s	$V_{IC} = 1 V_{r}$	- North	25°C	0.43	HO
SR	Cleve rate at unity gain	$R_L = 100 k\Omega$,	VI(PP) = 1 V	85°C	0.35	Mine
	Slew rate at unity gain	CL = 20 pF,	VILLE OFV	25°C	0.40	- V/µs
Vm	1001	See Figure 30	VI(PP) = 2.5 V	85°C	0.32	10
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	32	nV/√Hz
Paul	Maximum output quing bandwidth $V_{O} = V_{OH}$,	C _I = 20 pF,	25°C	55	141-	
BOM	Maximum output swing bandwidth	RL = 100 kΩ,	See Figure 30	85°C	45	- kHz
B. 80	Linite agin handwidth	V _I = 10 mV,	Ci = 20 pF,	25°C	525	A GOIN
B ₁	Unity-gain bandwidth	R _L = 100 kΩ,	See Figure 32	85°C	370	- kHz
	84 70 94	VI = 10 mV,	f = B ₁ ,	-40°C	43°	
φm	Phase margin	CL = 20 pF,	RL = 100 kΩ,	25°C 40°	40°	SVR WVD
		See Figure 32		85°C	38°	1

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						TLV23	334Y	2 3 4		
	PARAMETER	TEST C	ONDITIONS	V	DD = 3 \	/	V	DD = 5 \	1	UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	$V_{O} = 1 V,$ Rs = 50 Ω ,	VIC = 1 V RL = 100 kΩ		0.6	10	Jesilto Ju	1.1	10	mV
10	Input offset current (see Note 4)	V _O = 1 V,	V _{IC} = 1 V		0.1			0.1		pА
IIB	Input bias current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.6		- Incode of	0.6		pA
VICR	Common-mode input voltage range (see Note 5)	Namoenilure Common-mode	and the second se	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2	-	v
VOH	High-level output voltage	$V_{IC} = 1 V,$ $I_{OH} = -1 mA$	V _{ID} = 100 mV,	1.75	1.9	flow fundi	3.2	3.9	you	v
VOL	Low-level output voltage	$V_{IC} = 1 V,$ $I_{OL} = 1 mA$	V _{ID} = -100 mV,		115	150		95	150	mV
AVD	Large-signal differential voltage amplification	V _{IC} = 1 V, See Note 6	R _L = 100 kΩ,	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V,$ Rs = 50 Ω	V _{IC} = V _{ICR} min,	65	92	de Inpu	65	91	<u>ve</u>	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{IC} = 1 V,$ Rs = 50 Ω	V _O = 1 V,	70	94	10	70	94	Cal	dB
IDD	Supply current	V _O = 1 V, No load	VIC = 1 V,		320	1000	otori w	420	1120	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

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	V,

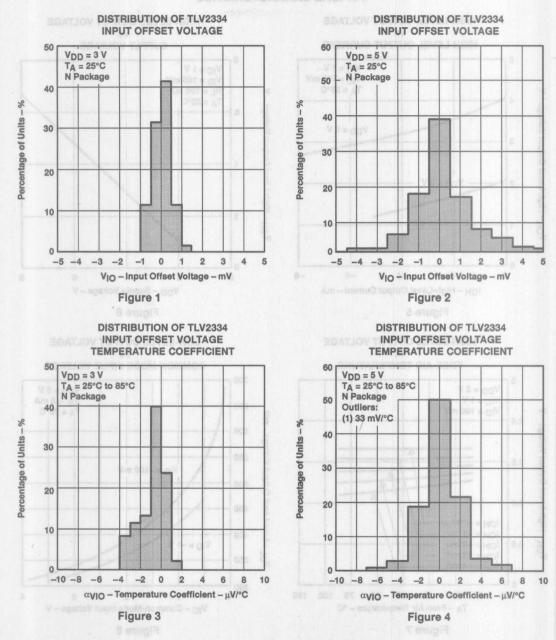


MAL TYP MAN XAM TYP MAN		FIGURE
VIO Input offset voltage	Distribution	1,2
aVIO Input offset voltage temperature co	efficient Distribution	3, 4
	vs Output current	5
VOH High-level output voltage	vs Supply voltage	6
6.0- S.0- S.0- S.0-	vs Temperature	hage eborn 7 orbi
2 2.3 4.2	vs Common-mode input voltage	8
	vs Temperature	9, 11
VOL Low-level output voltage	vs Differential input voltage	10
in the second	vs Low-level output current	12
A un lorge signal differential voltage am	vs Supply voltage	13
AVD Large-signal differential voltage am	vs Temperature	14
IB/IIO Input bias and offset currents	vs Temperature	15
VIC Common-mode input voltage	vs Supply current	16
ss Supply ourrent	vs Supply current	17
OL Low-level output voltage VD Large-signal differential voltage amplification B/IIO Input bias and offset currents IC Common-mode input voltage DD Supply current R Slew rate O(PP) Maximum peak-to-peak output voltage	vs Temperature	18
SR Slew rate	vs Supply voltage	19
	vs Temperature	20
VO(PP) Maximum peak-to-peak output volta	age vs Frequency	21
	vs Temperature	22
B1 Unity-gain bandwidth	vs Supply voltage	23
AVD Large-signal differential voltage am	plification vs Frequency	24, 25
	vs Supply voltage	26
om Phase margin	vs Temperature	27
	vs Load capacitance	28
Vn Equivalent input noise voltage	vs Frequency	29
Phase shift	vs Frequency	24,25

TYPICAL CHARACTERISTICS

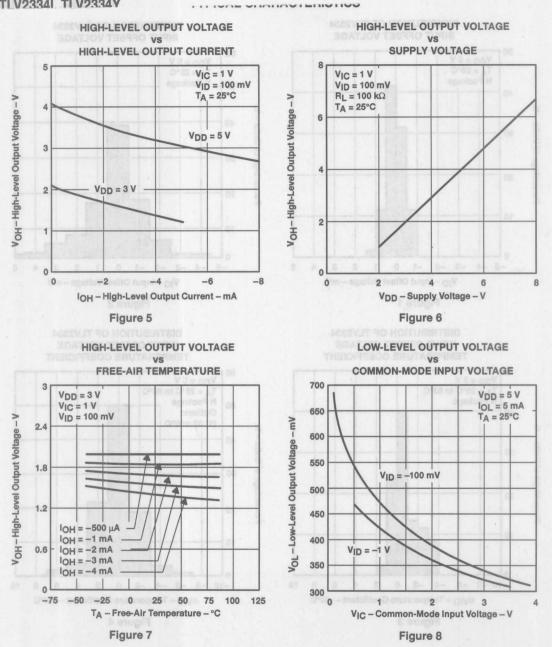


TYPICAL CHARACTERISTICS



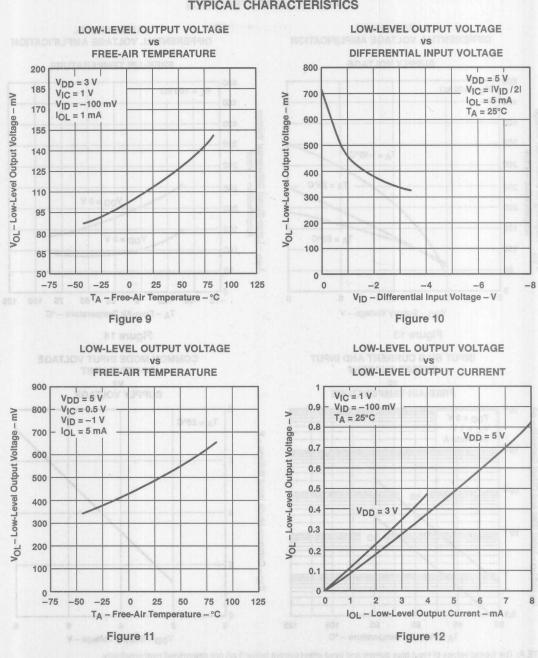


TI V23341 TI V2334V



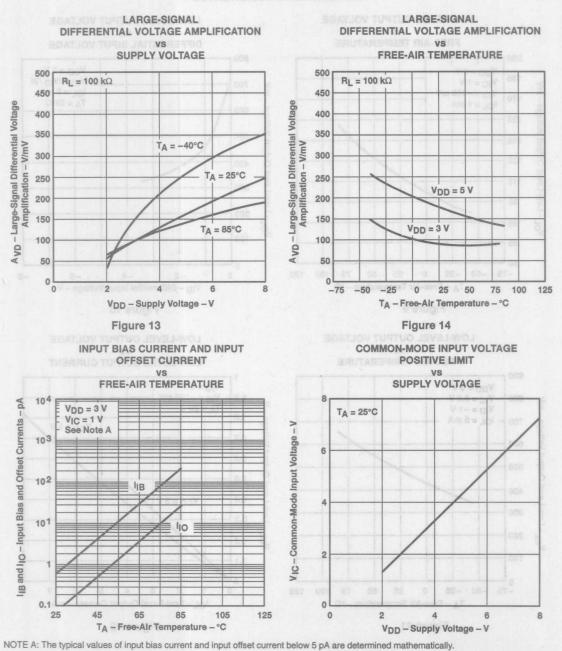
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TYPICAL CHARACTERISTICS





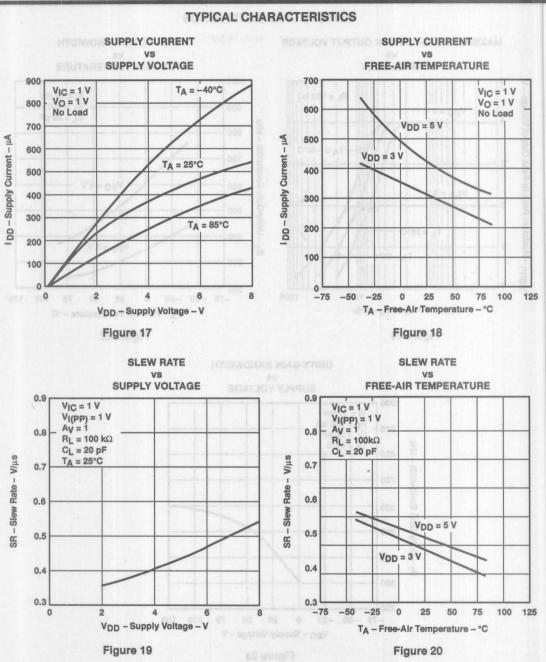
TYPICAL CHARACTERISTICS

Figure 15

Figure 16









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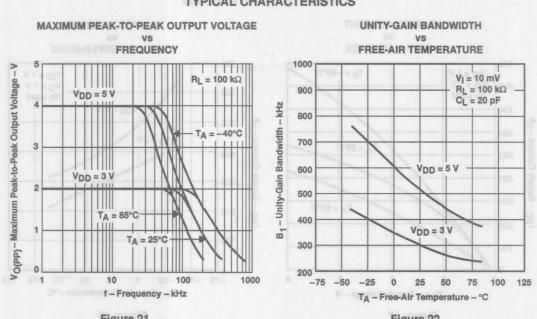
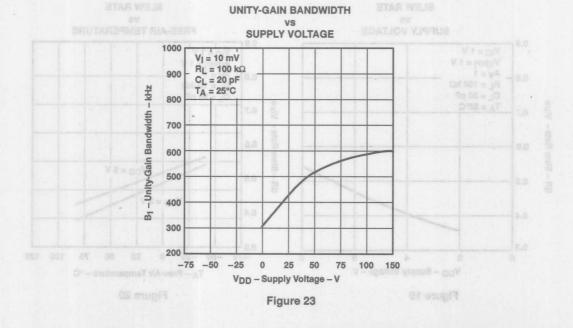


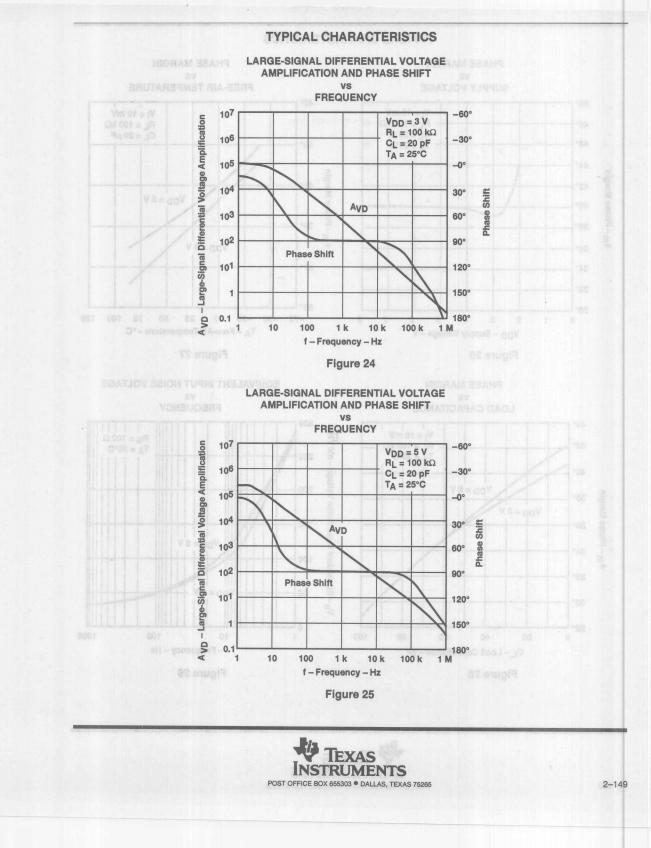


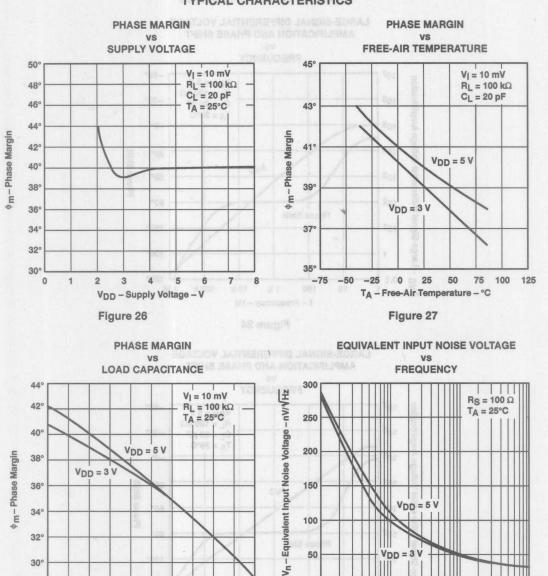
Figure 21





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0

1

100

10

f - Frequency - Hz

Figure 29

1000

TYPICAL CHARACTERISTICS

2-150

28°

0

20

40

Figure 28

CL - Load Capacitance - pF

60

80

100

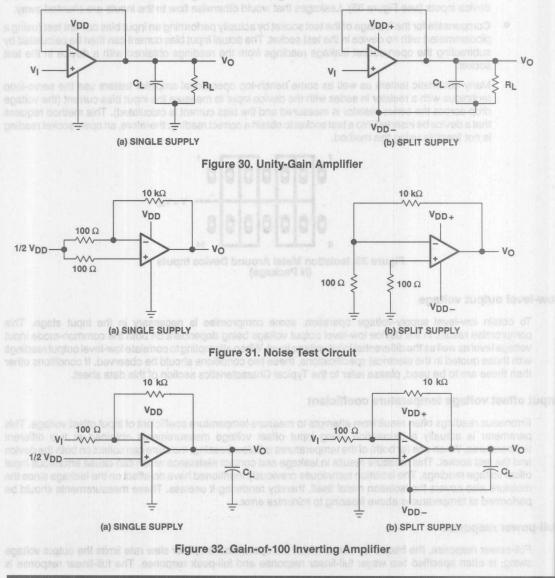
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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2334I is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.





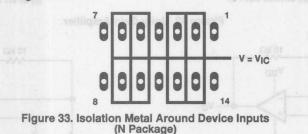
PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2334I operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.



low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is



PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

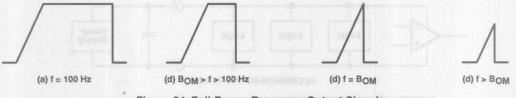


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2334I performs well using dualpower supplies (also called balanced or split supplies), the design is optimized for singlesupply operation. This includes an input commonmode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

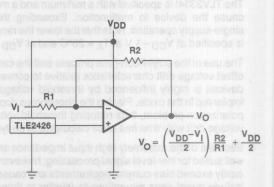


Figure 35. Inverting Amplifier With Voltage Reference

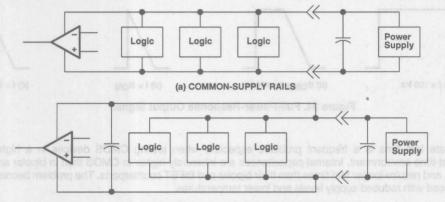


APPLICATION INFORMATION

single-supply operation (continued)

The TLV2334I works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)



input characteristics

The TLV2334I is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

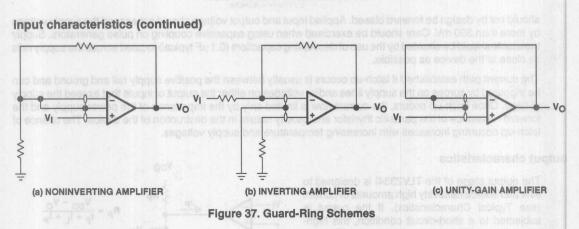
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2334I very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2334I is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level at the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



APPLICATION INFORMATION

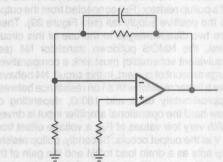


noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2334I results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.



electrostatic-discharge protection

Figure 38. Compensation for Input Capacitance

The TLV2334 incorporates an internal electro-static-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV23341 inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes



APPLICATION INFORMATION

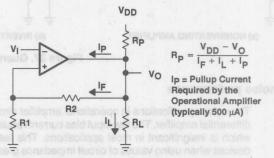
should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2334I is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this highcurrent capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2334I possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (RP) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60Ω and 180Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.





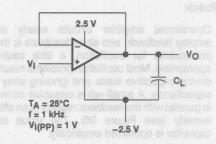


Figure 40. Test Circuit for Output Characteristics

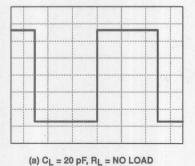
All operating characteristics of the TLV2334I are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

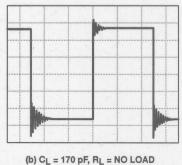
Because CMOS davices are susceptible to laten-up due to their inherent parasitiq invelsions, the TLV2334 nouts and outputs are designed to withstand – 100-mA surge currents without sustaining laten-up; however sonniques should be used to reduce the chance of laten-up whenever possible. Internal protection dicdes

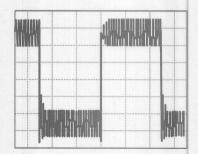


APPLICATION INFORMATION

output characteristics (continued)







(c) CL = 190 pF, RL = NO LOAD

Figure 41. Effect of Capacitive Loads

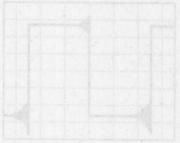


TILV23341, TLV23341, TLV23341, TLV23341 Lincmost" Low-Voltage Medalim-Power Quad Operational Amplifiens

APPLICATION INFORMATION

output characteristics (continued)





AL & NO LOAD

CAO LON # JR, NO LOAD

Neura 41. Effect of Canaolitve Load



description

The TLV2341 operational amplifier has been specifically developed for low-voltage, single-supply applications and is fully specified to operate over a voltage range of 2 V to 8 V. The device uses the Texas Instruments silicon-gate LinCMOS[™] technology to facilitate low-power, low-voltage operation and excellent offset-voltage stability. LinCMOS[™] technology also enables extremely high input impedance and low bias currents allowing direct interface to high-impedance sources.

The TLV2341 offers a bias-select feature, which allows the device to be programmed with a wide range of different supply currents and therefore different levels of ac performance. The supply current can be set at 17 μ A, 250 μ A, or 1.5 mA, which results in slew-rate specifications between 0.02 and 2.1 V/ μ s (at 3 V).

The TLV2341 operational amplifiers are especially well suited to single-supply applications and are fully specified and characterized at 3-V and 5-V power supplies. This low-voltage single-supply operation combined with low power consumption makes this device a good choice for remote, inaccessible, or portable battery-powered applications. The common-mode input range includes the negative rail.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2341 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883 C, Methods 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

AVAILABLE OPTIONS

		F	ACKAGED DE	VICES	OLUD
TA	VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
-40°C to 85°C	8 mV	TLV2341ID	TLV2341IP	TLV2341IPWLE	TLV2341Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2341IDR). The PW package is only available left-end taped and reeled (e.g., TLV2341IPWLE).

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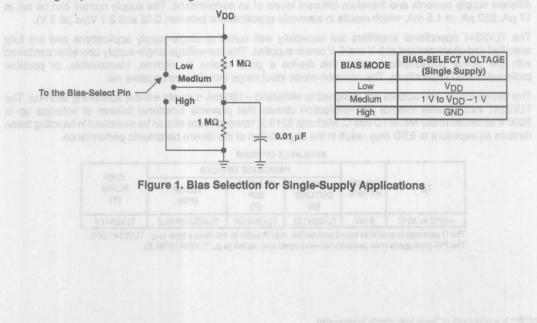
The TLV2342 offers a bias-select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

TYPICAL PARAMETER VALUES $T_A = 25^{\circ}C, V_{DD} = 3 V$			V 1-1		
		$\frac{\text{HIGH-BIAS}}{\text{R}_{\text{L}} = 10 \text{ k}\Omega}$	$\frac{\text{MEDIUM-BIAS}}{\text{R}_{L} = 100 \text{ k}\Omega}$	LOW-BIAS RL = 1 MΩ	UNIT
PD	Power dissipation	975	195	15	μW
SR	Slew rate	2.1	0.38	0.02	V/µs
Vn	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B ₁	Unity-gain bandwidth	790	300	27	kHz
φm.	Phase margin	46°	39°	`34°	
AVD	Large-signal differential voltage amplification	11	83	400	V/mV

Table 1. Effect	f Bias Selection	on Performance
-----------------	------------------	----------------

bias selection

Bias selection is achieved by connecting the bias-select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.





LinCMOS™ PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIERS SLOS110 - MAY 1992

high-bias mode

In the high-bias mode, the TLV2341 series feature low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation.

medium-bias mode

The TLV2341 in the medium-bias mode features a low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

In the low-bias mode, the TLV2341 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

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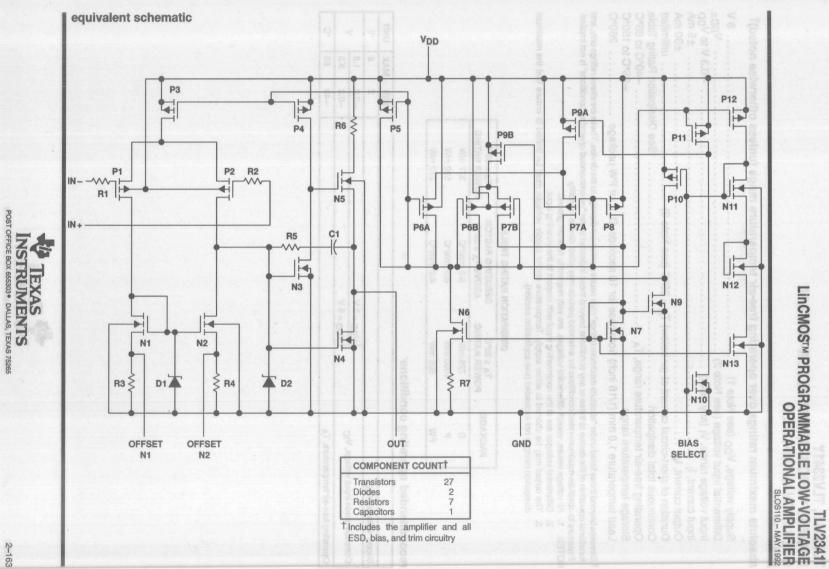
TLV2341I, TLV2341Y LinCMOSTM PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIERS SLOS110 - MAY 1992

TLV2341Y chip information

BONDING PAD ASSIGNMENTS data hata hata hata hata hata hata h Т. VDD OFFSET N1 (1) × iix. (7) (3) IN+ (6) OUT (2) Ŧ IN-(4) **OFFSET N2** (5) 48 GND (8) **BIAS SELECT** CHIP THICKNESS: 15 TYPICAL . **BONDING PADS: 4 × 4 MINIMUM** TJmax = 150°C TOLERANCES ARE ±10%. ALL DIMENSIONS ARE IN MILS. 55 1 իրիսիներիներիներիներիներիներին

This chip, when properly assembled, displays characteristics similar to the TLV23411. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{DD} (see Note 1)	
Differential input voltage (see Note 2)	V _{DD±}
Input voltage range, V _I (any input)	0.3 V to V _{DD}
Input current, I ₁	±5 mA
Output current, Io	±30 mA
Duration of short-circuit current at (or below) T _A = 25°C (see Note 3)	unlimited
Continuous total dissipation	. See Dissipation Rating Table
Operating free-air temperature range, TA	40°C to 85°C
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW	package 260°C

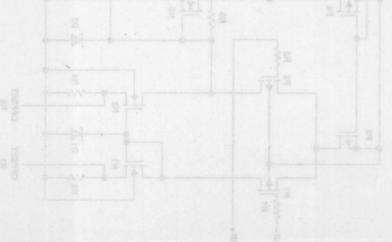
[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

	T∆ ≤ 25°C	DERATING FACTOR	TA = 85°C
PACKAGE	POWER RATING	ABOVE TA = 25°C	POWER RATING
D	725 mW	5.8 mW/°C	377 mW
Р	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, VDD		2	8	V
Common-mode input voltage, V _{IC}	V _{DD} = 3 V	-0.2	1.8	N
	$V_{DD} = 5 V$	-0.2	3.8	V
Operating free-air temperature, TA	7.0	-40	85	°C





TLV2341I, TLV2341Y LinCMOS™ PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIER SLOS110 - MAY 1992

HIGH-BIAS MODE

				TLV23411									
	PARAMETER	PARAMETER TEST CONDITIONS		V	DD = 3 \	/	V _{DD} = 5 V			UNIT			
	15 018	N I = requi	N.L.	MIN	TYP	MAX	MIN	TYP	MAX				
VIO	O Input offset voltage	$V_{O} = 1 V$, $V_{IC} = 1 V$, R _S = 50 Ω ,	25°C	* JR 1002	0.6	8	Map Vit	1.1	8	mV			
10	input one of voltage	$R_L = 10 k\Omega$	Full range	and a line		10			10				
αΛΙΟ	Average temperature of input offset voltage		25°C to 85°C	See	2.7			2.7		μV/°C			
lio	Input offset current (see Note 4)	$V_0 = 1 V$, $V_{IC} = 1 V$	25°C	= 181	0.1			0.1		pA			
10	input onset current (see Note 4)	VO = +V, $VIC = +V$	85°C	= 1V	22	1000		24	1000	ря			
IIB	Input bias current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	- A	0.6		(12) Mb	0.6	-Vielu	pA			
IB	input bias current (see Note 4)	10-10, VIC-10	85°C	806	175	2000	-	200	2000	μn			
	Common-mode input	= 8% L = 1 840,	25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2	ead ⁴	v			
VICR voltage range (see Note 5)	e acV ,emisso	Full range	-0.2 to 1.8	nisec	8 18 8	-0.2 to 3.8	doana	ng ci	v				
TINU	TLY2394U	VIC = 1 V,	25°C	1.75	1.9		3.2	3.7					
VOH	High-level output voltage	V _{ID} = 100 mV, I _{OH} = -1 mA			Full range	1.7			3			V	
	8.5 0.6	VIC = 1 V,	25°C	in B	120	150	alian uni	90	150				
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	i sea i		190			190	mV			
	Large-signal differential	VIC = 1 V,	25°C	3	11		5	23					
AVD	voltage amplification	$R_L = 10 k\Omega$, See Note 6	Full range	2			3.5		Nichola I	V/mV			
	0.00	$V_{O} = 1 V,$	25°C	65	78	hubned	65	80	nitestu				
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min,$ $R_S = 50 \Omega$					60			60			dB
Kovp	Supply-voltage rejection ratio	$V_{IC} = 1 V, V_{O} = 1 V,$	25°C	70	95		70	95		dB			
ksvr	(ΔV _{DD} /ΔV _{IO})	$R_{S} = 50 \Omega$	Full range	65			65			UB			
I(SEL)	Bias select current	VI(SEL) = 0	25°C	# 10	-1.2			-1.4	Pfagees	μА			
DD	Supply current	$V_{O} = 1 V, V_{IC} = 1 V,$	25°C	- suc	325	1500		675	1600	μА			
.00		No load	Full range			2000			2200	peri			

electrical characteristics at specified free-air temperature

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



TLV2341I, TLV2341Y LinCMOSTM PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIER SLOS110 - MAY 1992

HIGH-BIAS MODE

	APARSVIT	TEOT	TEST CONDITIONS		TLV23411	LINUT		
SR V _n B _{OM}	PARAMETER	TEST	ONDITIONS	TA	MIN TYP MAX	UNIT		
00		$V_{IC} = 1 V,$		25°C	2.1	V/us		
SK	Siew rate at unity gain RL = 10 kM, CL = 20 pr, See Figure 92		Slew rate at unity gain $R_L = 10 k\Omega$, $C_L = 20 pF$, 85°				1.7	η v/μs
vn	Equivalent input noise voltage	f = kHz, See Figure 93			25	nV/√Hz		
Davis	Maximum autout auting handwidth	Vo = VoH, CL = 20 pF,	25°C	170	kHz			
BOW	Maximum output swing bandwidth	$R_L = 10 k\Omega$,		85°C	145	KHZ		
-	22 1000 24 1000	V _I = 10 mV,	C _L = 20 pF,	25°C	790			
B ₁	Unity-gain bandwidth	RL = 10 K2, See Figure 94	R _L = 10 kΩ, See Figure 94	85°C	690	- kHz		
	E.0 5:0- E.0	VI = 10 mV,	f = B ₁ ,	-40°C	53°			
φm	Phase margin	C _L = 20 pF,		25°C	49°	1		
		See Figure 94		85°C	47°			

operating characteristics at specified free-air temperature, V_{DD} = 3 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V

	DADAMETED	1.9	TEOT	ONDITIONS	T	TLV2341I		
	PARAMETER		TEST	ONDITIONS	TA	MIN TYP MAX	UNIT	
			VIC = 1 V,	V	25°C	3.6		
00	Claurate at units ania		$R_L = 10 k\Omega$,	VI(PP) = 1 V	85°C	2.8		
SR	Slew rate at unity gain		C _L = 20 pF,	N 05 M	25°C	2.9	V/µs	
			See Figure 92 VI(PP) = 2.5 V 85 f = 1 kHz, R _S = 100 Ω, 25 See Figure 93 25	85°C	2.3			
Vn	Equivalent input noise volt	age		R _S = 100 Ω,	25°C	25	nV/√Hz	
Part	Maximum autout auting ha	n du ci dèla	VO = VOH, CL	CL = 20 pF,	25°C	320	kHz	
BOM	Maximum output swing ba	nawiath	$R_L = 10 k\Omega$,	CL = 20 pF, See Figure 92	85°C	250		
P.	Lipity goin bandwidth		V _I = 10 mV,	CL = 20 pF,	25°C	1.7	MU	
B ₁	Unity-gain bandwidth		$R_L = 10 k\Omega$,	See Figure 94	85°C	1.2	MHz	
- 00	66		V _I = 10 mV,	f = B ₁ ,	-40°C	49°	71800	
φm	Phase margin		CL = 20 pF,	R _L = 10 kΩ,	25°C	46°	1.19(2)	
			See Figure 94		85°C	43°		

Full range is -40°C to 85°C.

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TLV2341I, TLV2341Y LinCMOS™ PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIER SLOS110 - MAY 1992

HIGH-BIAS MODE

	3RUDR			TLV2341I						
	PARAMETER	TEST CONDITIONS		V _{DD} = 3 V			V _{DD} = 5 V			UNIT
		nuitudintmi i	Intelic	MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage				0.6	8	to level r	1.1	8	mV
10	Input offset current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$			0.1			0.1		pА
IIB	Input bias current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$			0.6			0.6		pА
VICR	Common-mode input voltage range (see Note 5)	 eutérequel ex eutérequel éx 		-0.2 to 2	-0.3 to 2.3	diov log	-0.2 to 4	-0.3 to 4.2	Vol	v
VOH	High-level output voltage	$V_{IC} = 1 V$, $V_{ID} = 100 mV$, $I_{OH} = -1 mA$		1.75	1.9		3.2	3.7	mal	V
VOL	Low-level output voltage	$V_{IC} = 1 V$, $V_{ID} = -100 mV$ $I_{OL} = 1 mA$		- and a second se	120	150	us asid h	90	150	mV
AVD	Large-signal differential voltage amplification	$V_{IC} = 1 V$, $R_L = 10 k\Omega$, See Note 6		3	11	huqni eb	50	23	OIV	V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V, \qquad V_{IC} = V_{ICR} min \\ R_{S} = 50 \Omega$	l,	65	78		65	80	00	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$			70	95		70	95	1	dB
II(SEL)	Bias select current	VI(SEL) = 0		man then a da	-1.2		and the second	-1.4		μA
IDD	Supply current	$V_{O} = 1 V$, $V_{IC} = 1 V$, No load			325	1500	et cleavy	675	1600	μА

electrical characteristics, $T_A = 25^{\circ}C$

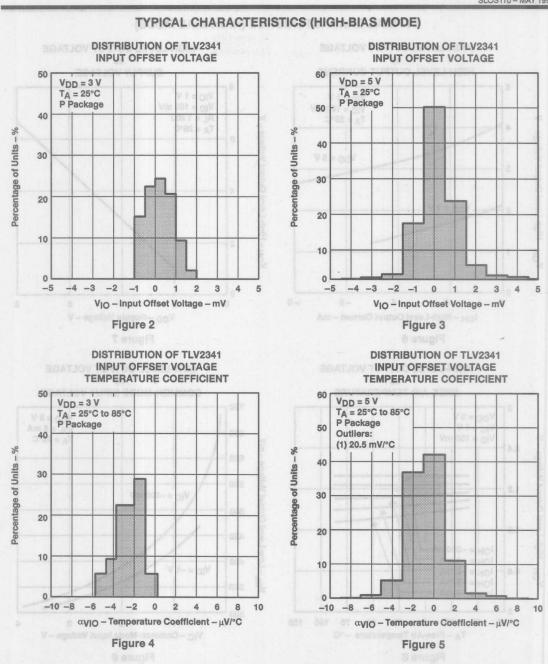
NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



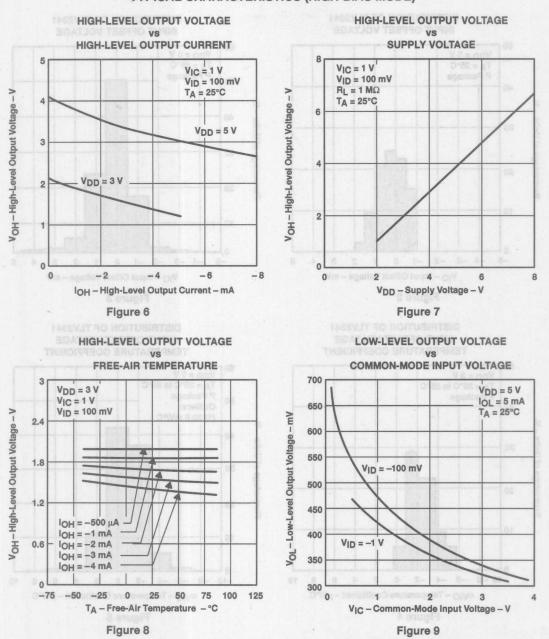
	TLY2341		FIGURE
VIO	Input offset voltage	Distribution	2,3
ανιο	Input offset voltage temperature coefficient	Distribution	4,5
		vs Output current	6
Vон	High-level output voltage	vs Supply voltage	7
- F.		vs Temperature	8
3.	8.0	vs Common-mode input voltage	9
ε.	0- 20+ 80- 80-	vs Temperature	10, 12
VOL	Low-level output voltage	vs Differential input voltage	stol/ etti) epi
		vs Low-level output current	13
	9.7 9.7	vs Supply voltage	14
AVD	Large-signal differential voltage amplification	vs Temperature	15
IIB/IIO	Input bias and offset currents	vs Temperature	16
VIC	Common-mode input voltage	vs Supply voltage	17
		vs Supply voltage	18
DD	Supply current	vs Temperature	19
SR	Olaw rate	vs Supply voltage	20
SH	Slew rate	vs Temperature	21
	Bias select current	vs Supply voltage	22
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	23
	ra 10001 885	vs Temperature	24
B ₁	Unity-gain bandwidth	vs Supply voltage	25
AVD	Large-signal differential voltage amplification	vs Frequency	26, 27
	V 8.1 of V 6.	vs Supply voltage	28
Þm	Phase margin	vs Temperature	29
		vs Load capacitance	30
Vn	Equivalent input noise voltage	vs Frequency	31
	Phase shift	vs Frequency	26,27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)





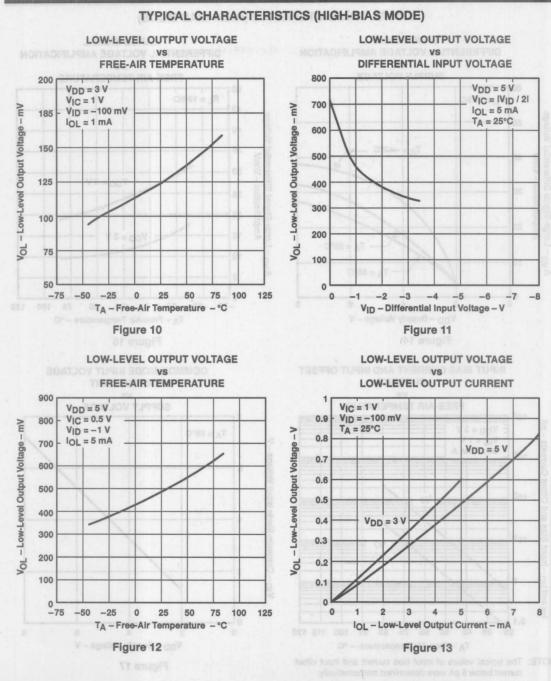




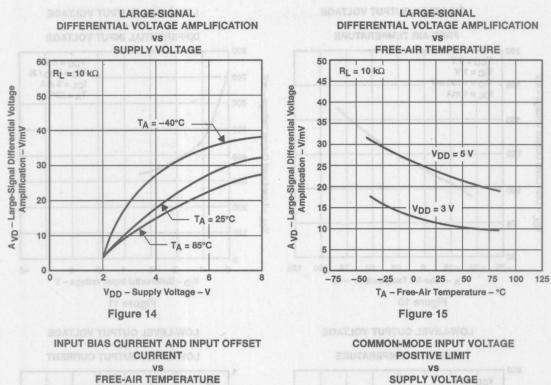
TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)











>-

6

0

0

2

4

VDD - Supply Voltage - V

Figure 17

6

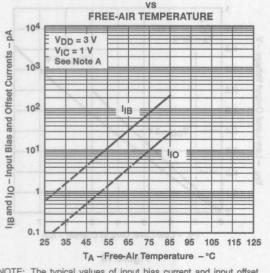
8

- Common-Mode Input Voltage

VIC

TA = 25°C

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)



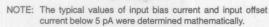
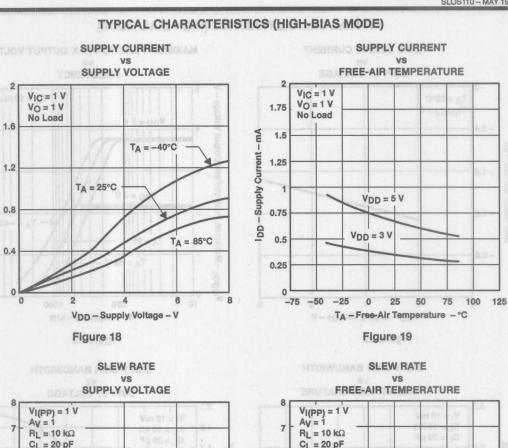


Figure 16



I DD - Supply Current - mA

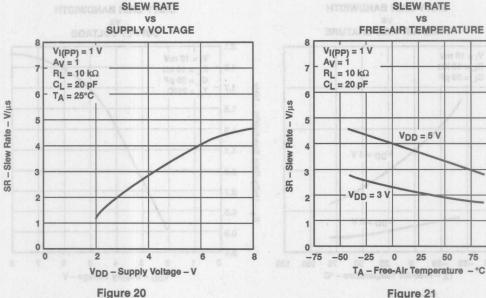
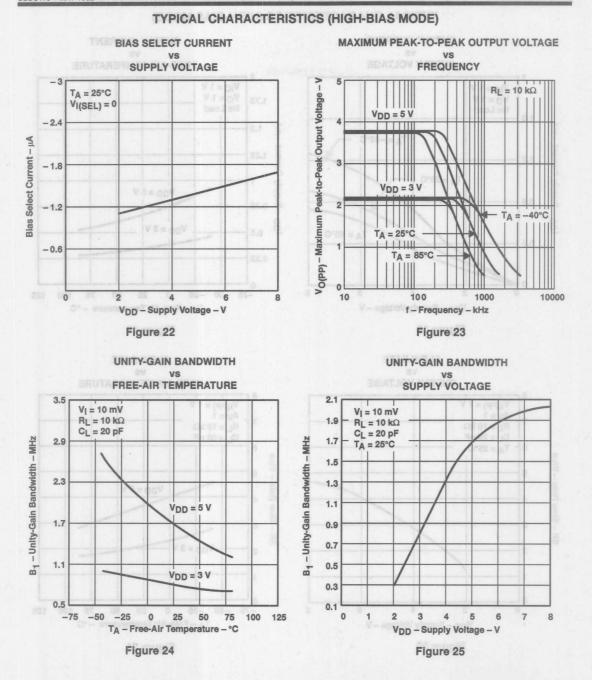


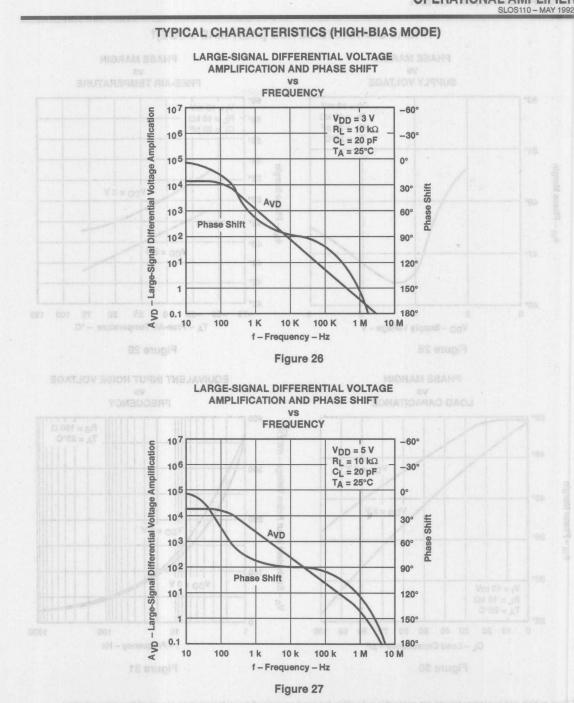
Figure 21

75 100 125

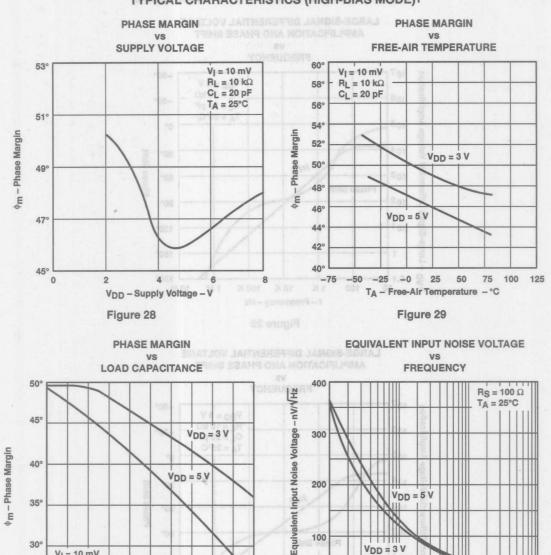












TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)[†]

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

90 100



100

0

1

- un

VDD = 3 V

11111

10

f - Frequency - Hz

Figure 31

100

1000

30°

25°

 $V_I = 10 \text{ mV}$

 $R_L = 10 k\Omega$

TA = 25°C

0 10 20 30 40 50 60 70 80

Figure 30

CL - Load Capacitance - pF

MEDIUM-BIAS MODE

		Sector Sector	no tear			TLV2	3411	anate		
	PARAMETER	TEST CONDITIONS	TAT	V	DD = 3 \	/	V	DD = 5 \	1	UNIT
	8°C 0.38	(PP) = (PP)	V. NI	MIN	TYP	MAX	MIN	TYP	MAX	
Vio	Input offset voltage	$V_{O} = 1 V$, $V_{IC} = 1 V$, Rs = 50 Ω ,	25°C	111	0.6	8	ning yan	1.1	8	mV
VIO	input onset voltage	$R_L = 100 \text{ k}\Omega$	Full range	10(-)		10	asine	and bush	10	niv
αΛΙΟ	Average temperature coefficient of input offset voltage	30.05 -	25°C to 85°C	Sag I	1			1.7		μV/°C
luc	Input offset current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	=]A	0.1	Annual Contract	N SAKE THE	0.1	CILCUMER .	Aq
10	input onset current (see Note 4)	vO = v, $vIC = v$	85°C	VIII	22	1000		24	1000	рд
IIB	Input bias current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	- (A	0.6		1 page 1 card	0.6		pA
IB	input bias current (See Note 4)	v0=+v, vic=+v	85°C	- NI	175	2000		200	2000	PA
		(# 1001kG),	25°C	-0.2 to	-0.3 to		-0.2 to	-0.3 to		v
	Common-mode input		20-0	2	2.3		4	4.2		V
VICR	voltage range (see Note 5)	erature, V _{DD} =	Full range	-0.2 to 1.8	peol	e in e	-0.2 to 3.8	10816	ing ch	V
11794	XAM SYT HOL AT	V _{IC} = 1 V,	25°C	1.75	1.9		3.2	3.9		
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $I_{OH} = -1 \text{ mA}$	Full range	1.7	1.0		3	0.0		V
V/µts	20 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$V_{IC} = 1 V_{i}$	25°C		115	150	ity gain	95	150	- 91
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	200	110	190			190	mV
stillion	Large-signal differential	V _{IC} = 1 V,	25°C	25	83	epallo	25	170	Equive	
AVD	voltage amplification	RL = 100 kΩ, See Note 6	Full range	15	-		15		-	V/mV
		$V_0 = 1 V$,	25°C	65	92	CALIFIC A REACT	65	91		-10
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min,$ R _S = 50 Ω	Full range	60			60	rusid nisp	Unity-r	dB
ksvr	Supply-voltage rejection ratio	V _{IC} = 1 V, V _O = 1 V,	25°C	70	94		70	94		dB
SVH	(ΔVDD/ΔVIO)	R _S = 50 Ω	Full range	65			65	ciprati.	Phases	u.D
I(SEL)	Bias select current	VI(SEL) = 0	25°C	6ea	-100			-130		nA
	Supply current	$V_{O} = 1 V, V_{IC} = 1 V,$	25°C		65	250		105	280	
IDD	Supply current	No load	Full range			360		-	400	μA

electrical characteristics at specified free-air temperature

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

	DADAMETED	TEOT	ONDITIONO	-	TLV2341I	115.07
	PARAMETER	TEST	CONDITIONS	TA	MIN TYP MAX	UNIT
0.0	XAM 9YT MM XAM 9YT	VIC = 1 V,		25°C	0.38	Mue
SR	Slew rate at unity gain	$R_L = 100 k\Omega$, See Figure 92	CL = 20 pF,	85°C	0.29	V/µs
Vn	Equivalent input noise voltage	f = kHz, See Figure 93	R _S = 100 Ω,	25°C	32	nV/√Hz
P		Vo = VoH,	C1 = 20 pF,	25°C	34	
BOM	Maximum output swing bandwidth	RL = 100 kΩ,	See Figure 92	85°C	32	kHz
-	22 1000 24 1000	V _I = 10 mV,	C _I = 20 pF,	25°C	300	
B ₁	Unity-gain bandwidth	R _L = 100 kΩ,	See Figure 94	85°C	235	kHz
	2000 2000 2000 200	$V_{I} = 10 \text{ mV},$	f = B ₁ ,	-40°C	42°	
φm	Phase margin	CL = 20 pF,	RL = 100 kΩ,	25°C	39°	
		See Figure 94		85°C	36°	

operating characteristics at specified free-air temperature, V_{DD} = 5 V

	DADAMETED		TEAT	ONDITIONO	-	TLV23411	
	PARAMETER		TEST	CONDITIONS	TA	MIN TYP MAX	UNIT
V.	The second of the second s		$V_{IC} = 1 V,$	Ver Gut	25°C	0.43	HO
00	Class water at such sacia		$R_L = 100 \text{ k}\Omega$	VI(PP) = 1 V	85°C	0.35	Ma
SR	Slew rate at unity gain		$C_{L} = 20 \text{ pF},$	N	25°C	0.40	V/µs
	001		See Figure 92	VI(PP) = 2.5 V	85°C	0.32	.10
Vn	Equivalent input noise vo	ltage	f =1 kHz, See Figure 93	R _S = 100 Ω,	25°C	telmenette (32 javenna)	nV/√H:
Barr	Mauina autout autou	an duri alth	Vo = VoH,	C1 = 20 pF,	25°C	55	Lel In
BOM	Maximum output swing b	andwidth	$R_L = 100 \text{ k}\Omega,$	See Figure 92	85°C	45	kHz
80	Lipity goin bandwidth		V _I = 10 mV,	CL = 20 pF,	25°C	525	- Helle
B ₁	Unity-gain bandwidth		R _L = 100 kΩ,	See Figure 94	85°C	370	kHz
85	10 DI		$V_{I} = 10 \text{ mV},$	f = B ₁ ,	-40°C	43°	RUR
φm	Phase margin		CL = 20 pF,	RL = 100 kΩ,	25°C	40°	
Aa	- 130	-100	See Figure 94	0 = (.5)	85°C	38°	(JB8)
Aa	106 280	66 260	26/10	VI-ON VI	- QV	Supply curital	an

Full range is - 40°C to 86°C.

TTS: 4 The trained viewing of insul blag and and

This range also socies to each inout individually.

At Von = 5 V, Yo = 0.25 V to 2 V; at Von = 0.4, Voi = 0.5 V to 1

MEDIUM-BIAS MODE

electrical characteristics, T_A = 25°C

						TLV	23411		1.1.1	
	PARAMETER	TEST C	ONDITIONS	V	DD = 3 \	oitage V	In the N	DD = 5	I OVIT	UNIT
		noltudi		MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	$V_{O} = 1 V,$ R _S = 50 Ω ,	$V_{IC} = 1 V,$ $R_L = 100 k\Omega$		0.6	8	o lovel-r	1.1	8	mV
10	Input offset current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.1			0.1		pА
IB	Input bias current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.6			0.6	-	pА
VICR	Common-mode input voltage range (see Note 5)	enutemani Tuqni kilos att	में २५ Q ४४	-0.2 to 2	-0.3 to 2.3	diov tuq	-0.2 to 4	-0.3 to 4.2	VOL	v
VOH	High-level output voltage	V _{IC} = 1 V, I _{OH} = -1 mA	V _{ID} = 100 mV,	1.75	1.9	in the second	3.2	3.9	CVA	V
VOL	Low-level output voltage	$V_{IC} = 1 V,$ $I_{OL} = 1 mA$	V _{ID} = -100 mV,		115	150	n ssid I	95	150	mV
AVD	Large-signal differential voltage amplification	VIC = 1 V, See Note 6	R _L = 100 kΩ,	25	83	tuqril eh	25	170	Vic	V/m\
CMRR	Common-mode rejection ratio	$V_{O} = 1 V,$ R _S = 50 Ω	$V_{IC} = V_{ICR}min$,	65	92		65	91	001	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{O} = 1 V,$ $R_{S} = 50 \Omega$	VIC = 1 V,	70	94	-	70	94		dB
II(SEL)	Bias select current	VI(SEL) = 0		anatinu 1	-100	no. ind sta	and structures	-130	a.avil	nA
DD	Supply current	V _O = 1 V, No load	V _{IC} = 1 V,		65	250	niep-v	105	280	μА

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

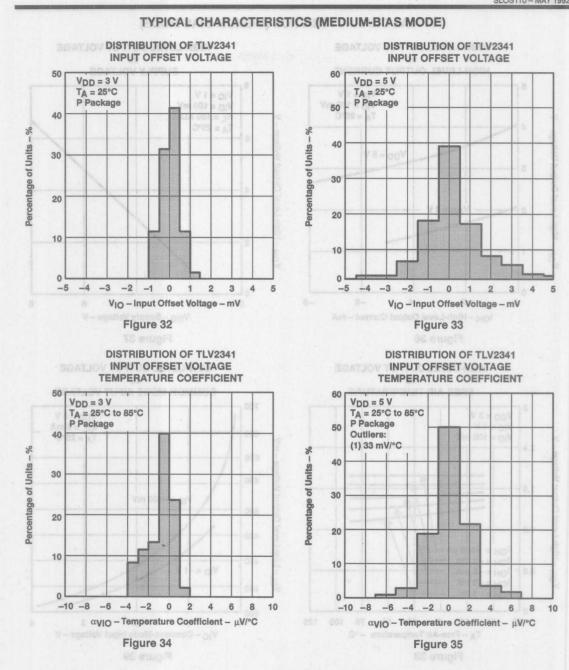


			FIGURE
VIO	Input offset voltage	Distribution	32, 33
ανιο	Input offset voltage temperature coefficient	Distribution	34, 35
	8 80 N	vs Output current	36
VOH	High-level output voltage	vs Supply voltage	37
		vs Temperature	38
	Q 0.0	vs Common-mode input voltage	39
6.	-0.2 -0.3 -0.2 -0	vs Temperature	40, 42
VOL	Low-level output voltage	vs Differential input voltage	41
	The second process of the second proces of t	vs Low-level output current	43
8		vs Supply voltage	44
AVD	Large-signal differential voltage amplification	vs Temperature	45
IB/IO	Input bias and offset currents	vs Temperature	46
VIC	Common-mode input voltage	vs Supply voltage	47
		vs Supply voltage	48
DD	Supply current	vs Temperature	49
0.0	Oleverate	vs Supply voltage	50
SR	Slew rate	vs Temperature	51
-	Bias select current	vs Supply current	52
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	53
6 21	01	vs Temperature	54
B ₁	Unity-gain bandwidth	vs Supply voltage	55
AVD	Large-signal differential voltage amplification	vs Frequency	56, 57
	Valat Va	vs Supply voltage	58
¢m	Phase margin	vs Temperature	59
		vs Load capacitance	60
Vn	Equivalent input noise voltage	vs Frequency	61
	Phase shift	vs Frequency	56.57

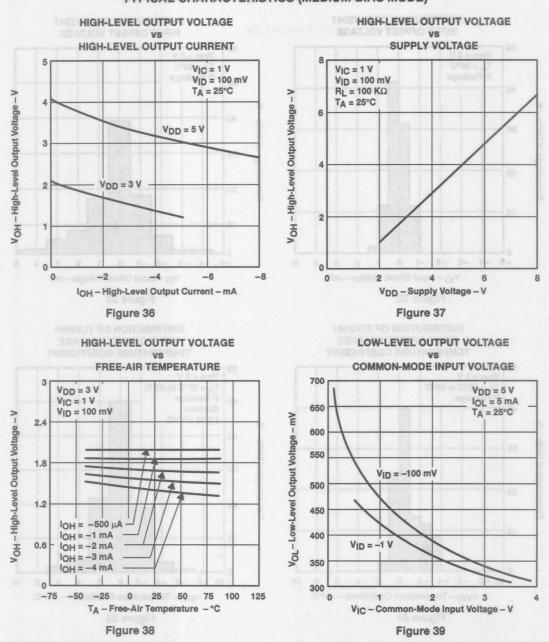
TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)



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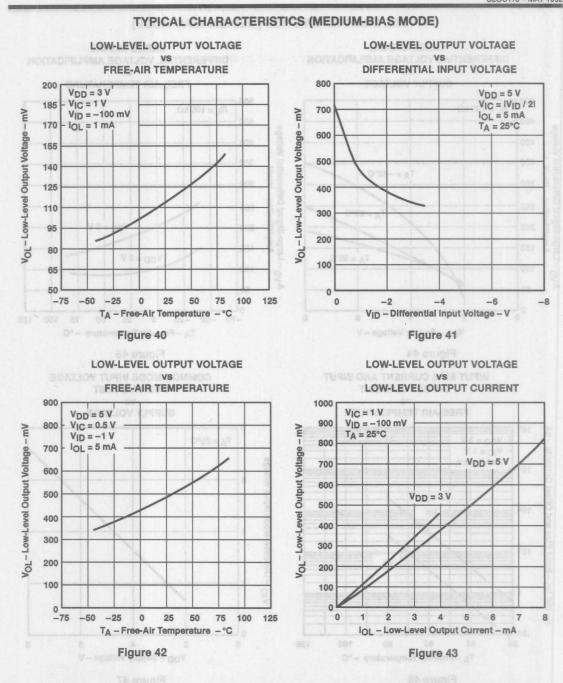




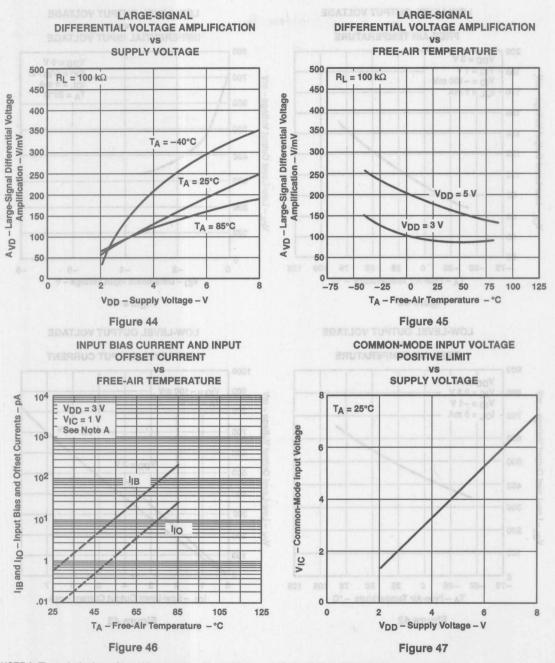
TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)



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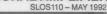


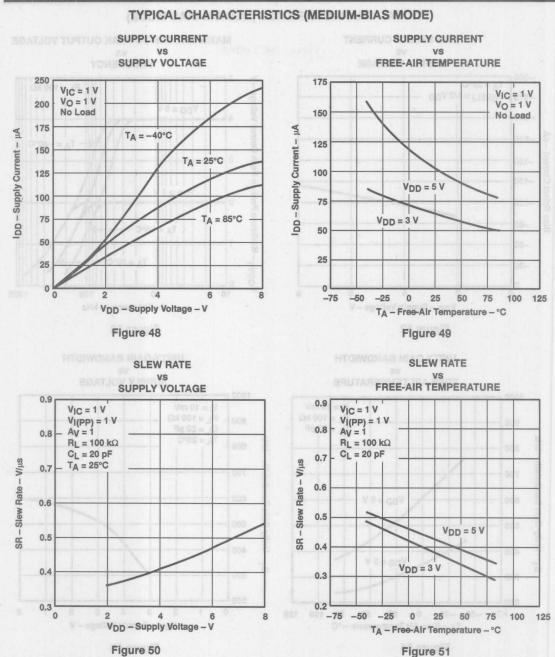


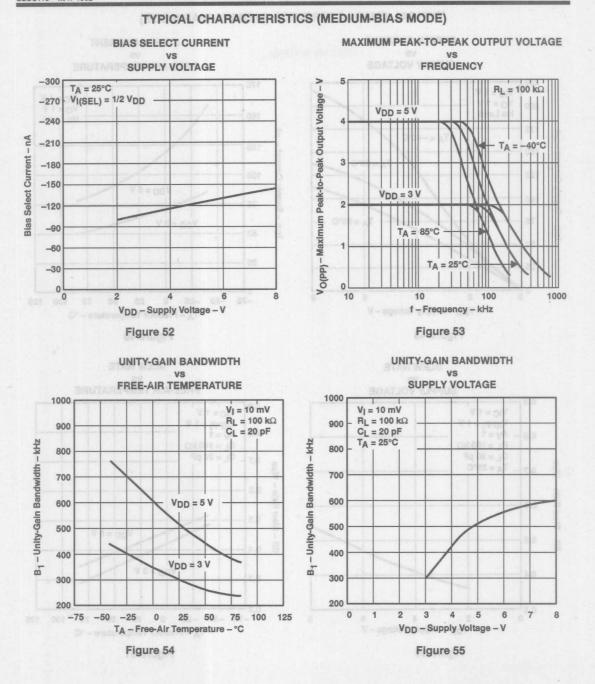
TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.









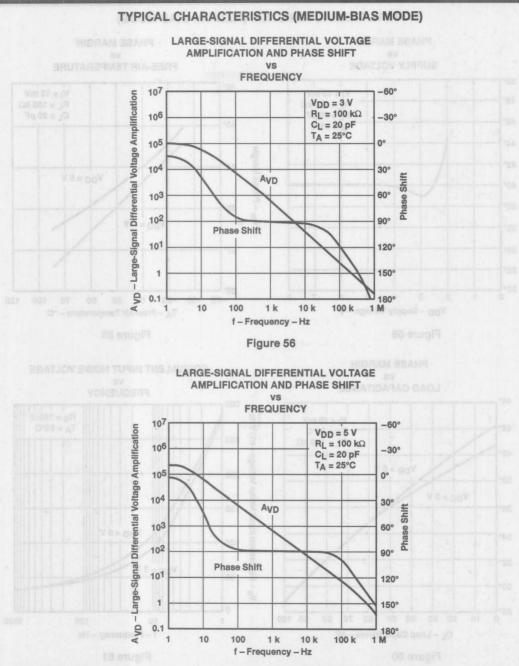
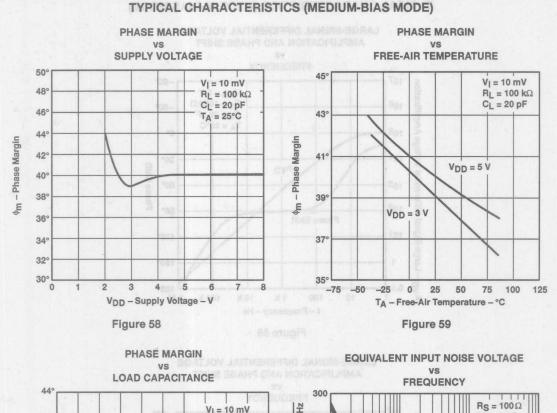
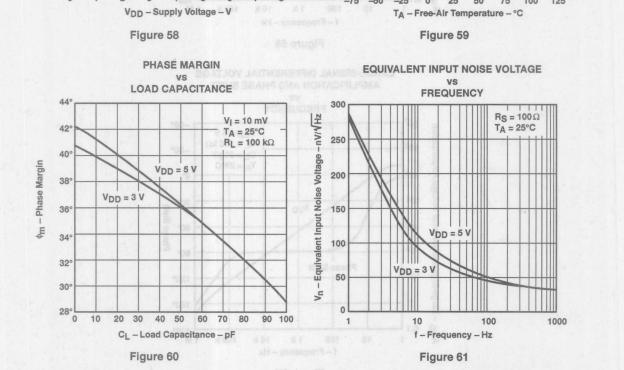


Figure 57





LOW-BIAS MODE

		and a state	an main			TLV2	3411			
	PARAMETER	TEST CONDITIONS	TAT	V	DD = 3 \	/	V	DD = 5 V	1	UNIT
	50.0	V tow/ap	V VI	MIN	TYP	MAX	MIN	TYP	MAX	
Vio	Input offset voltage	$V_{O} = 1 V$, $V_{IC} = 1 V$, R _S = 50 Ω ,	25°C	19 19 1 9 19 2	0.6	8	UHBE YES	1.1	8	mV
•10	input onoci tokago	$R_L = 1 M\Omega$	Full range			10	and and a	and track	10	
αΛΙΟ	Average temperature of input offset voltage		25°C to 85°C	1.052 F	1			1.1		μV/°C
lic	Input offset current (see Note 4)	$V_0 = 1 V$, $V_{10} = 1 V$	25°C		0.1			0.1		pA
10	input onset current (see Note 4)	$v_0 = v$, $v_0 = v$	85°C	I walk	22	1000		24	1000	pA
IIB	Input bias current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	- 181	0.6			0.6	1	pA
IB	mput bias current (See Note 4)	v0=+v, v10=+v	85°C	(and	175	2000		200	2000	pri
		DM I H	PI Re C	-0.2	-0.3		-0.2	-0.3	Pjanso	
	Commune modelinguit	1 Junior March	25°C	to 2	to 2.3		to 4	to 4.2		V
VICR	Common-mode input voltage range (see Note 5)	iereture, V _{DD} = I	Full range	-0.2 to 1.8	illano	e is e	-0.2 to 3.8	doava	lo gri	V
THU	XAN AVT HIM	$V_{IC} = 1 V_{i}$	25°C	1.75	1.9		3.2	3.8		
VOH	High-level output voltage	V _{ID} = 100 mV, I _{OH} = -1 mA	Full range	1.7			3			V
RUN	200	V _{IC} = 1 V,	25°C	C . 0.2	115	150	urső An	95	150	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	380.1		190			190	mV
SPINA	Large-signal differential	V _{IC} = 1 V,	25°C	50	400	spalle	50	520	Equiva	
AVD	voltage amplification	R _L = 1 MΩ, See Note 6	Full range	50			50		- interests	V/m\
	810 J	V _O = 1 V,	25°C	65	88		65	94		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min,$ RS = 50 Ω	Full range	60	1		60	yain baha	Unity-s	dB
koup	Supply-voltage rejection ratio	$V_{IC} = 1 V, V_{O} = 1 V,$	25°C	70	86		70	86		dB
KSVR	$(\Delta V_{DD}/\Delta V_{IO})$	R _S = 50 Ω	Full range	65			65	nigrain	Pinkan	ub
II(SEL)	Bias select current	VI(SEL) = 0	25°C	11663	10			65		nA
	Cupply ourrent	$V_{O} = 1 V, V_{IC} = 1 V,$	25°C		5	17		10	17	
DD	Supply current	No load	Full range			27		1.1.2.1	27	μA

electrical characteristics at specified free-air temperature

[†] Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O(PP) = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



LOW-BIAS MODE

	TARGEVER.	TEAT	CONDITIONO	-	T	LV23411		LINUT
	PARAMETER	TEST	CONDITIONS	TA	MIN	TYP	MAX	UNIT
	TYP MAX'S MIN TYP MAX	$V_{IC} = 1 V,$		25°C		0.02		
SR	Slew rate at unity gain	$R_{L} = 1 M\Omega,$ See Figure 92	СL = 20 рн,	85°C	epis	0.02	to sugni	V/µs
Vn	Equivalent input noise voltage	f = kHz, See Figure 93	R _S = 100 Ω,	25°C	to ender	68	(cates) A	nV/√Hz
- WA		Vo = VoH,	CI = 20 pF,	25°C	ංරුන	2.5	lo iutori	L.L.
BOM	Maximum output swing bandwidth	$R_L = 1 M\Omega$,	See Figure 92	85°C		2		kHz
-	1000 1000 1000	$V_{I} = 10 \text{ mV},$	C ₁ = 20 pF,	25°C		27		Let la
B ₁	Unity-gain bandwidth	$R_L = 1 M\Omega$,	See Figure 94	85°C	La thirty	21	Le annie	kHz
100	176 2000 2000 2000	$V_{I} = 10 \text{ mV},$	f = B ₁ ,	-40°C		39°		-
φm	Phase margin	CL = 20 pF,		25°C		34°		
		See Figure 94		85°C		28°		1

operating characteristics at specified free-air temperature, V_{DD} = 3 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V

		TEOT	CONDITIONS	-	TLV2341I	
	PARAMETER	TEST	CONDITIONS	TA	MIN TYP MAX	UNIT
V		VIC = 1 V,	V	25°C	0.03	HO
00	Class sate at units agin	$R_L = 1 M\Omega$,	VI(PP) = 1 V	85°C	0.03	V/µs
SR	Slew rate at unity gain	CL = 20 pF,	N 051	25°C	0.03	ν/μs
		See Figure 92	VI(PP) = 2.5 V	85°C	0.02	
Vn	Equivalent input noise voltage	f =1 kHz, See Figure 93	R _S = 100 Ω,	25°C	68	nV/√Hz
Davis	Manimum and a start has a start with	Vo = VoH,	C ₁ = 20 pF,	25°C	5	Let la
BOM	Maximum output swing bandwidth	$R_L = 1 M\Omega$,	See Figure 92	85°C	4	kHz
B. 80	I Inity anis baseduidth	V _I = 10 mV,	CL = 20 pF,	25°C	85	Let la
B ₁	Unity-gain bandwidth	$R_L = 1 M\Omega$,	See Figure 94	85°C	55	kHz
1	36 70 86	V _I = 10 mV,	f = B ₁ ,	-40°C	38°	RVR
φm	Phase margin	CL = 20 pF,	$R_L = 1 M\Omega$,	25°C	34°	25.46
		See Figure 94		85°C	28°	112103

Full raives to -- 40°C to 85°C.

TER- A The fundad welling of the

This statistical second data to another include a local data

LOVED = OV VE = OV VE VERV SEV VED = OOV V J = OOVIA .



LOW-BIAS MODE

electrical characteristics, T_A = 25°C

-	38UQM					TLV2	341Y			
	PARAMETER	TEST CON	IDITIONS	V	DD = 3 \	/ Agailor	V	DD = 5 \	I OIV	UNIT
		nohudista	G hok	MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	V _O = 1 V, R _S = 50 Ω,	$V_{IC} = 1 V,$ $R_L = 1 M\Omega$		0.6	8	o lavál a	1.1	8	mV
10	Input offset current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.1			0.1		pА
IIB	Input bias current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.6			0.6		pA
VICR	Common-mode input voltage range (see Note 5)	Temperatura Diferential Riput y		-0.2 to 2	-0.3 to 2.3	diav tuqi	-0.2 to 4	-0.3 to 4.2	Jov	v
VOH	High-level output voltage	V _{IC} = 1 V, I _{OH} = -1 mA	V _{ID} = 100 mV,	1.75	1.9		3.2	3.8	Auto	V
VOL	Low-level output voltage	$V_{IC} = 1 V,$ $I_{OL} = 1 mA$	V _{ID} = -100 mV,	toto	115	150	t binut ex	95	150	mV
AVD	Large-signal differential voltage amplification	V _{IC} = 1 V, See Note 6	R _L = 1 MΩ,	50	400	nadur og	50	520	Vic	V/m\
CMRR	Common-mode rejection ratio	$V_{O} = 1 V,$ R _S = 50 Ω	$V_{IC} = V_{ICR}min$,	65	88	and the second second	65	94	-00	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{DD} = 3 V \text{ to } 5 V,$ $V_{O} = 1 V,$	$V_{IC} = 1 V,$ Rs = 50 Ω	70	86	and the second	70	86	88	dB
II(SEL)	Bias select current	VI(SEL) = 0		and they be	10	an otala	a designed	65	and I	nA
IDD	Supply current	V _O = 1 V, No load	V _{IC} = 1 V,		5	17	d niep-s	10	17	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

XAS INSTRUMENTS

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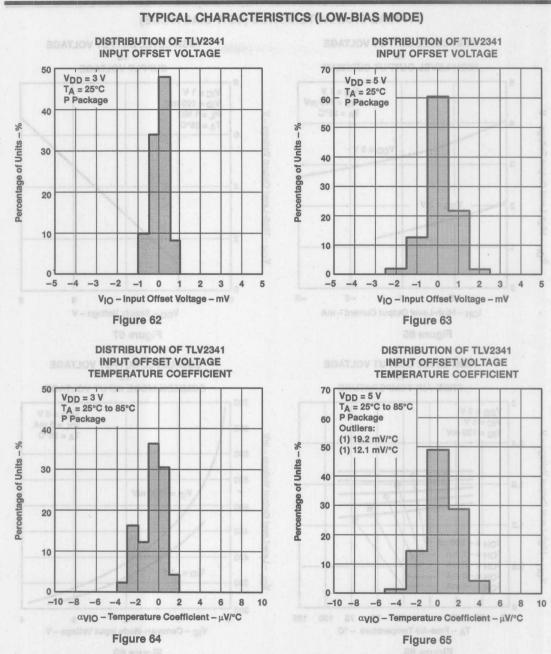
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	TLVESKIY		FIGURE
VIO	Input offset voltage	Distribution	62, 63
ανιο	Input offset voltage temperature coefficient	Distribution	64, 65
	NI NI	vs Output current	66
Vон	High-level output voltage	vs Supply voltage	67
		vs Temperature	68
a.	0 0.0 V F	vs Common-mode input voltage	69
	-0.2 -0.3 -0.2 -0	vs Temperature	70, 72
VOL	Low-level output voltage	vs Differential input voltage	71 00
		vs Low-level output current	73
4		vs Supply voltage	74
AVD	Large-signal differential voltage amplification	vs Temperature	75
IIB/IIO	Input bias and offset currents	vs Temperature	76
VIC	Common-mode input voltage	vs Supply voltage	77
		vs Supply voltage	78
DD	Supply current	vs Temperature	79
SR	Slew rate	vs Supply voltage	80
SR	Siew rate	vs Temperature	81
	Bias select current	vs Supply current	82
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	83
1 0		vs Temperature	84
B ₁	Unity-gain bandwidth	vs Supply voltage	85
AVD	Large-signal differential voltage amplification	vs Frequency	86, 87
6	V010V8	vs Supply voltage	88
[¢] m	Phase margin	vs Temperature	89
		vs Load capacitance	90
Vn	Equivalent input noise voltage	vs Frequency	91
	Phase shift	vs Frequency	86,87

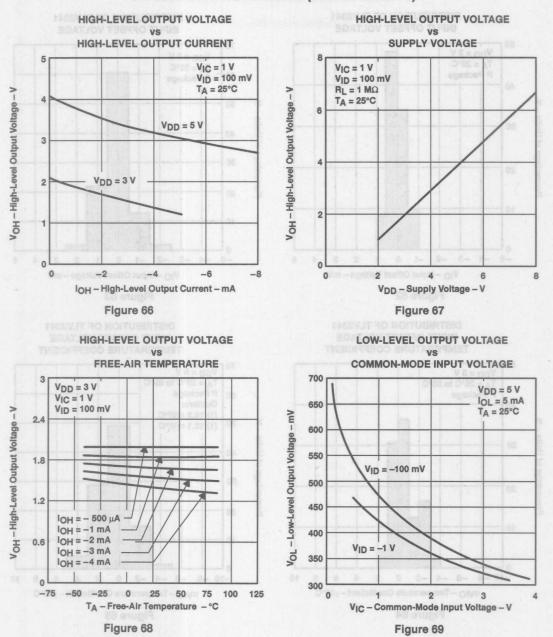
TYPICAL CHARACTERISTICS (LOW-BIAS MODE)





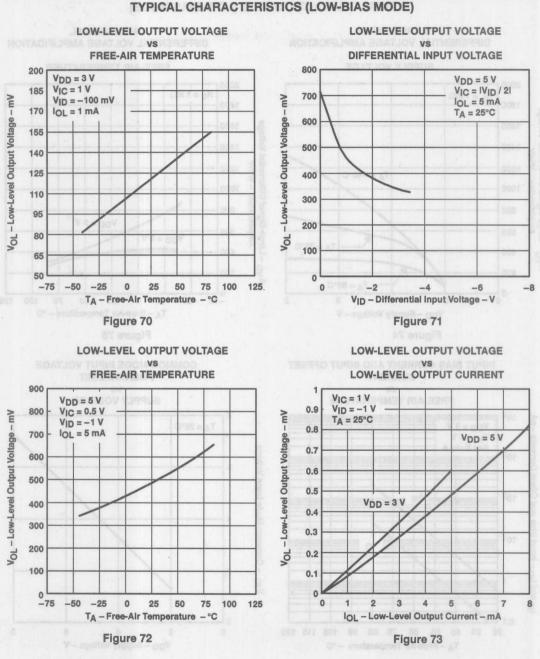




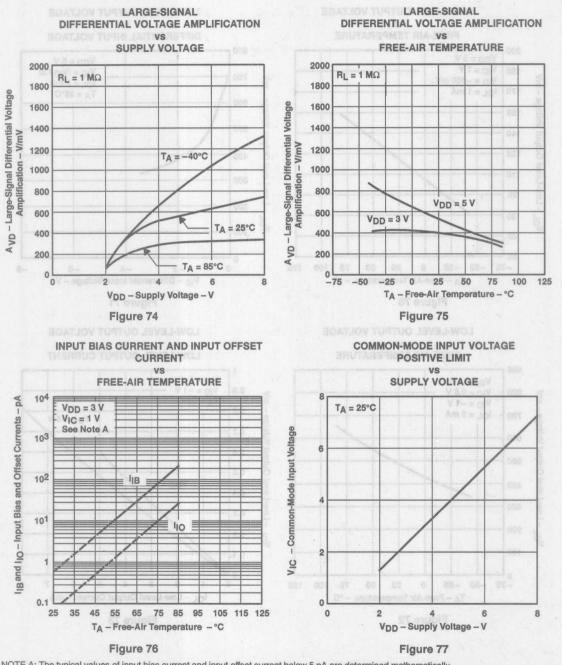


TYPICAL CHARACTERISTICS (LOW-BIAS MODE)









TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.



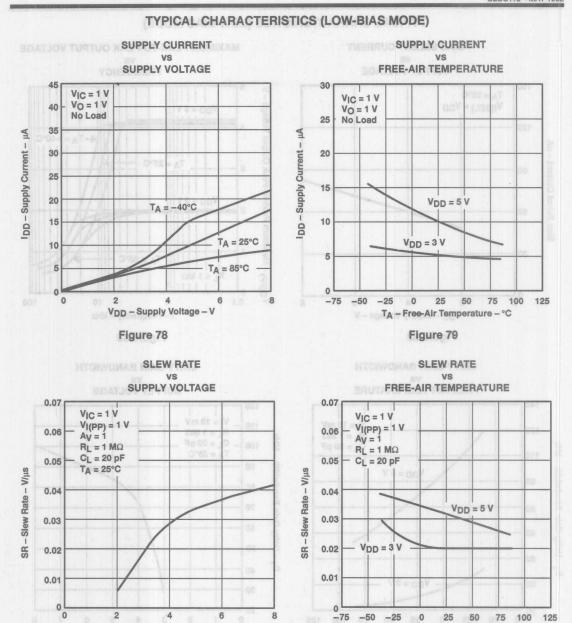


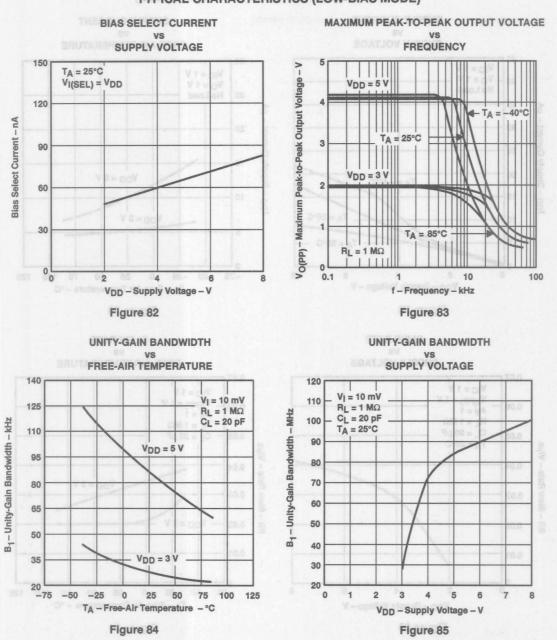
Figure 81

TA - Free-Air Temperature - °C



VDD - Supply Voltage - V

Figure 80



TYPICAL CHARACTERISTICS (LOW-BIAS MODE)



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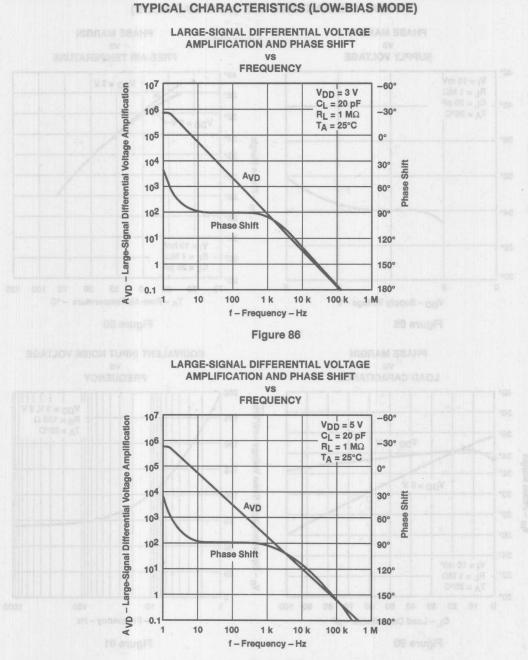
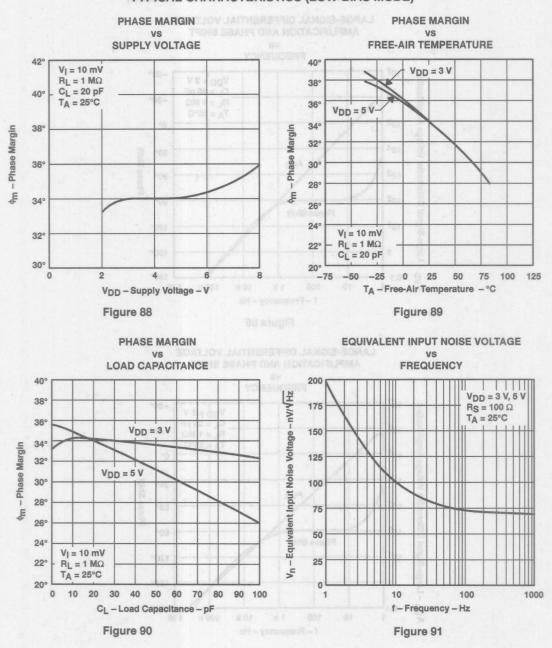


Figure 87



TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

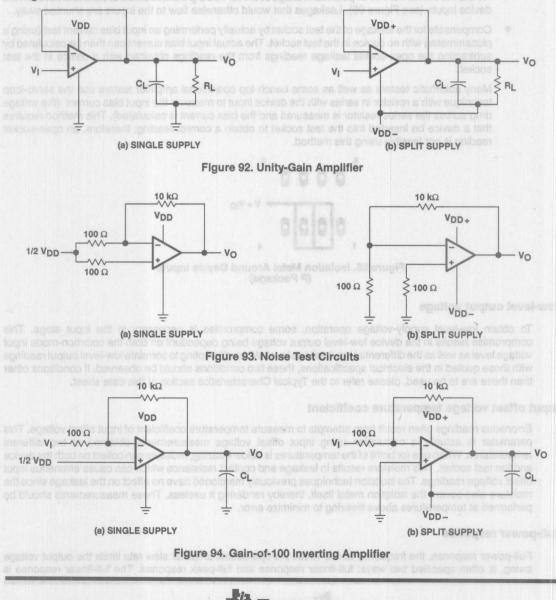


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PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2341 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2341 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 95). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a
 picoammeter) with no device in the test socket. The actual input bias current can then be calculated by
 subtracting the open-socket leakage readings from the readings obtained with a device in the test
 socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

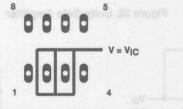


Figure 95. Isolation Metal Around Device Inputs (P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

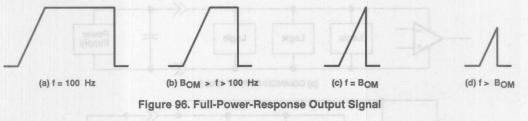
Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is



PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 92. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 96). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



test time

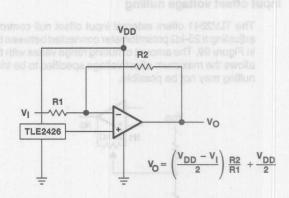
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2341 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to V_{DD}/2, while consuming very little power and is suitable for supply voltages of greater than 4 V.







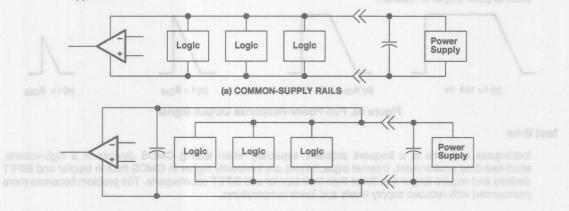
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APPLICATION INFORMATION

single-supply operation (continued)

The TLV2341 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 98); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
 - Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive
 decoupling is often adequate; however, RC decoupling may be necessary in high-frequency
 applications.

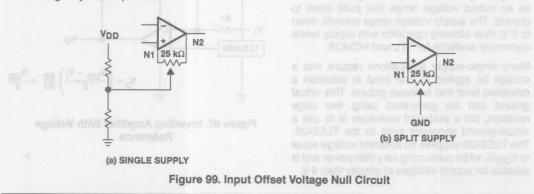


(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)

Figure 98. Common Versus Separate Supply Rails

input offset voltage nulling

The TLV2341 offers external input offset null control. Nulling of the input offset voltage can be achieved by adjusting a 25-k Ω potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 99. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range allows the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.





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APPLICATION INFORMATION

bias selection

input charatanistics (continued

Bias selection is achieved by connecting the bias-select pin to one of the three voltage levels (see Figure 100). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.

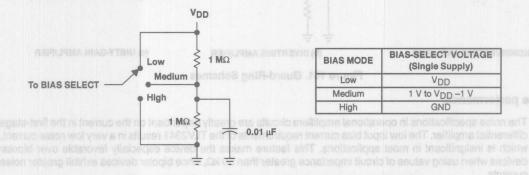


Figure 100. Bias Selection for Single-Supply Applications

input charac teristics

The TLV2341 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2341 good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2341 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 95 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 101).

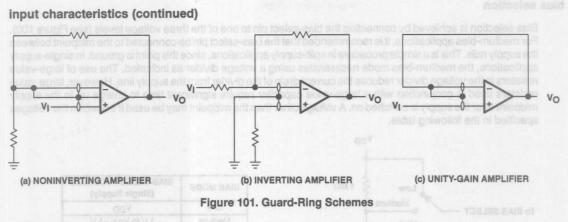
The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

Because CMOB devices are susceptible to latch-up due to their infrarent parasilio invitators, the TLV2541 inputs and output are designed to withstand – 150-mA surge currents without existaining (atch-up; nowever, techniques should be used to reduce the chance of latch-up whanever possible, tritemat protection diodes should not by



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APPLICATION INFORMATION



noise performance

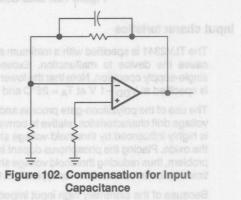
The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2341 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 102). The value of this capacitor is optimized empirically.

electrostatic-discharge protection

The TLV2341 incorporates an internal electrostatic-discharge (ESD)-protection circuit that



prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2341 inputs and output are designed to withstand – 100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by



APPLICATION INFORMATION

design be forward biased. Applied input and output voltage should not exceed the supply voltage by more that 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2341 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2341 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 103). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60Ω and 180Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

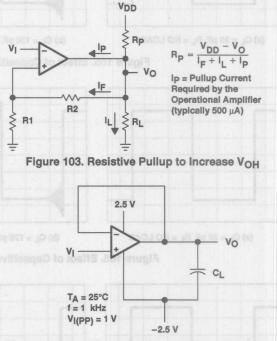


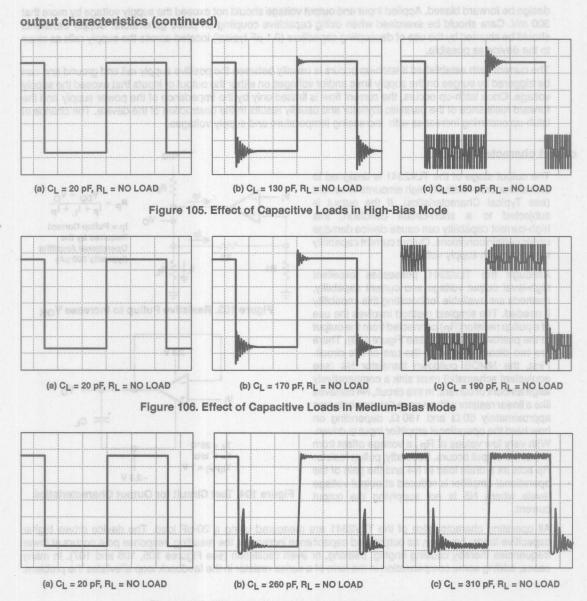
Figure 104. Test Circuit for Output Characteristics

All operating characteristics of the TLV2341 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 105, 106 and 107). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



TLV2341I, TLV2341Y LinCMOSTM PROGRAMMABLE LOW-VOLTAGE OPERATIONAL AMPLIFIER SLOS110 - MAY 1992









D OR P PACKAGE

- Wide Range of Supply Voltages Over Specified Temperature Range: -40°C to 85°C...2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range
 Extends Below the Negative Rail and
 Latch-Up to V_{DD} –1 V at 25°C
 - Output Voltage Range Includes Negative Rail
 - High Input Impedance ... 10¹² Ω Typical
 - ESD-Protection Circuitry
 - Designed-In Latch-Up Immunity

description

The TLV2342 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2342 was developed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2342 has a typical slew rate of 2.1 V/µs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of -40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

Low-voltage and low-power operation has been made possible by using Texas Instruments silicon-

gate LinCMOS[™] technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2342 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

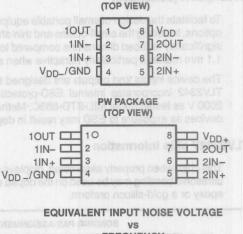
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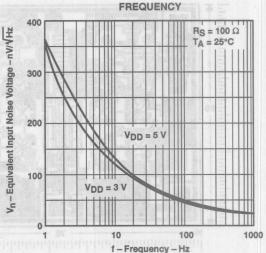
		CKAGED DEVICE	S		
TA	T _A V _{IO} max AT 25°C SMALL OUT (D)		PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
-40°C to 85°C	9 mV	TLV2342ID	TLV2342IP	TLV2342IPWLE	TLV2342Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2342IDR). The PW package is only available left-end taped and reeled (e.g., TLV2342IPWLE).

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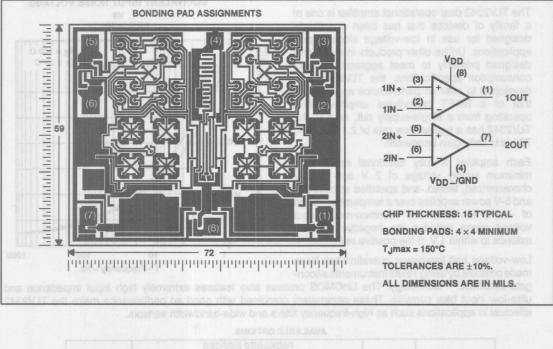
description (continued)

To facilitate the design of small portable equipment, the TLV2342 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

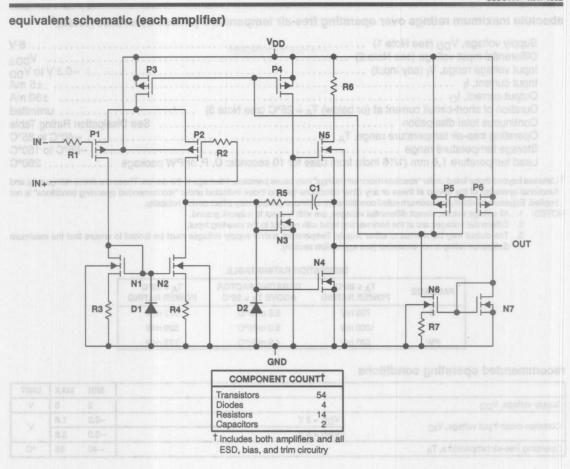
The device inputs and outputs are designed to withstand -100-mA currents without sustaining latch-up. The TLV2342 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

TLV2342Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2342I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.









absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{DD} (see Note 1)	
Differential input voltage (see Note 2) Input voltage range, V _I (any input)	
Input current, I	
Output current, Io	
Duration of short-circuit current at (or below) $T_A = 25^{\circ}C$ (see Note 3)	
Continuous total dissipation See	
Operating free-air temperature range, TA	
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package	ge 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at the noninverting input with respect to the inverting input.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE										
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING							
D	725 mV	5.8 mW/°C	377 mW							
P	1000 mV	8.0 mW/°C	520 mW							
PW	525 mV	4.2 mW/°C	273 mW							

recommended operating conditions

	Tenneisburg	MIN	MAX	UNIT
Supply voltage, VDD	Diodes 4	2	8	V
	V _{DD} = 3 V	-0.2	1.8	N
Common-mode input voltage, VIC	V _{DD} = 5 V	-0.2	3.8	V
Operating free-air temperature, TA	E3D, bies, and bim okculity	-40	85	°C



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	1 IEARSVIT I	a tore of the second				TLV2	3421			
	PARAMETER	TEST CONDITIONS	TAT	V _{DD} = 3 V		1	V _{DD} = 5 V		1	UNIT
		Virepje tV	NT.	MIN	TYP	MAX	MIN	TYP	MAX	
Vio	Input offset voltage	$V_{O} = 1 V$, $V_{IC} = 1 V$, $R_{S} = 50 \Omega$,	25°C	A JA	0.6	9	rilag yila	1.1	9	mV
		$R_L = 10 k\Omega$	Full range			11			11	
ανιο	Average temperature coefficient of input offset voltage	Gi = 20 df.	25°C to 85°C	See	2.7			2.7		μV/°C
lic	Input offset current (see Note 4)	$V_0 = 1 V$, $V_{IC} = 1 V$	25°C	m jR	0.1	A MONTOPOL	a service and	0.1		
10	input onset current (see Note 4)	vO = i v, v C = i v	85°C	m Wi -	22	1000		24	1000	pA
IIB	Input bias current (see Note 4)	$V_0 = 1 V$, $V_{IC} = 1 V$	25°C	= 1913	0.6		Magreen	0.6	- Course	pA
IB	mput bias current (see Hote 4)	v0=+v, v1C=+v	85°C	- della	175	2000		200	2000	μA
	Common-mode input	common-mode input	25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2	Philips	v
VICR	voltage range (see Note 5)	perature, V _{OD} = I	Full range	-0.2 to 1.8	Aloeq	e 16 e	-0.2 to 3.8	toener	io gri	V
Linni	MIN TYP BAX	V _{IC} = 1 V,	25°C	1.75	1.9		3.2	3.7		
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $I_{OH} = -1 \text{ mA}$	Full range	1.7			3			V
milth	5°C 2.9	V _{IC} = 1 V,	25°C		120	150	nisg yn	90	150	1
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	005		190			190	mV
SHIWA	Large-signal differential	VIC = 1 V,	25°C	3	11	apatio	5	23	Equiva	
AVD	voltage amplification	R _L = 10 kΩ, See Note 6	Full range	2			3.5	-1	nikold	V/m\
	280	V _O = 1 V,	25°C	65	78		65	80		
CMRR	$ \begin{array}{l} \mbox{Common-mode rejection ratio} & \mbox{V}_{IC} = \mbox{V}_{ICRmin}, \\ \mbox{R}_{S} = 50 \ \Omega \\ \end{array} $	$V_{IC} = V_{ICR}min,$ $R_S = 50 \Omega$	Full range	60			60	rved hing	eglint0	dB
kaura	Supply-voltage rejection ratio	$V_{IC} = 1 V, V_{O} = 1 V,$	25°C	70	95		70	95		dD
ksvr	$(\Delta V_{DD}/\Delta V_{IO})$	R _S = 50 Ω	Full range	65			65	niguson	Phase	dB
	Supply ourrant	$V_{O} = 1 V$, $V_{IC} = 1 V$,	25°C	800	0.65	3		1.4	3.2	
IDD	Supply current	No load	Full range			4		1.1.1.5	4.4	mA

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



	DADAMETED	av.ar	TERTO	ONDITIONS	-	TLV2342I	UNIT
	PARAMETER		TESTO	UNDITIONS	TA	MIN TYP MAX	
0.0	XAM 9YT HIM	TYP MAK	$V_{IC} = 1 V,$	$V_{I(PP)} = 1 V,$ $C_{L} = 20 \text{ pF},$	25°C	2.1	Mus
SR	Slew rate at unity gain		$R_L = 10 k\Omega$, See Figure 30	С <u>L</u> = 20 рг,	85°C	1.7	V/µs
Vn	Equivalent input noise v	voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	25	nV/√Hz
Passard.		have doubtly	Vo = VoH,	$C_{I} = 20 \text{pF},$	25°C	170	L.L.
BOM	Maximum output swing	bandwidth	$R_L = 10 k\Omega$,	See Figure 30	85°C	145	- kHz
-	24	22 1900	V _I = 10 mV,	C ₁ = 20 pF,	25°C	790	
B ₁	Unity-gain bandwidth		$R_L = 10 k\Omega$,	See Figure 32	85°C	690	kHz
-	200 2000	176 2000	V _I = 10 mV,	f = B1,	-40°C	53°	
φm	Phase margin		$C_{L} = 20 \text{ pF},$	$R_L = 10 k\Omega$,	25°C	49°	1
			See Figure 32		85°C	47°	1

operating characteristics at specified free-air temperature, V_{DD} = 5 V

	DADAMETED	TEST	ONDITIONS	TA	TLV2342I	LINUT
	PARAMETER	TEST C	TEST CONDITIONS		MIN TYP MAX	UNIT
V	In the second	V _{IC} = 1 V,	N	25°C	3.6	8 HQ
SR	Claus rate at units rain	$R_{I} = 10 \text{ k}\Omega,$	VI(PP) = 1 V	85°C	2.8	Mus
	Slew rate at unity gain	$C_L = 20 \text{ pF},$		25°C	2.9	- V/μs
Vm	l ogi	See Figure 30	VI(PP) = 2.5 V	85°C	2.3	- 10
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	25	nV/√H
Paul		Vo = VoH,	CL = 20 pF,	25°C	320	kHz
BOM	Maximum output swing bandwidth	$R_L = 10 k\Omega$,	See Figure 30	85°C	250	KHZ
B. 60	Linit, goin bondwidth	V _I = 10 mV,	CL = 20 pF,	25°C	cite e 1.7 chine	C RHM
B ₁	Unity-gain bandwidth	$R_L = 10 k\Omega$,	See Figure 32	85°C	1.2	- kHz
-	85 70 95	Vi = 10 mV.	f = B ₁ ,	-40°C	49°	8 AV8
φm	Phase margin	C _L = 20 pF,	$R_L = 10 k\Omega$,	25°C	46°	NV6
		See Figure 32		85°C	43°	

Full races is ~40°C to 86°

ES: 4. The typical values of injust bias outrant and input offect current below 5 pA are determined mathematics 5. This range also applies to each input individually.

A 91, 01 A 90 × 6A 'A 6 × 90 A 88 'A 8 64 A 680 × 6A 'A 0 × 60 A 36



A1 11	F 100		CRARK.	1000	R (1)	a second of
		SI	OS11	4-	M	AV 19

	PARAMETER	TEST CONDITIONS		V	DD = 3 \	/	V _{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN TYP		MAX	
VIO	Input offset voltage	$V_{O} = 1 V,$ R _S = 50 Ω ,	$V_{IC} = 1 V,$ $R_L = 10 k\Omega$		0.6	9	r tigetto t	1.1	9	mV
10	Input offset current (see Note 4)	V _O = 1 V,	VIC = 1 V		0.1			0.1	1212	рА
IIB	Input bias current (see Note 4)	V _O = 1 V,	VIC = 1 V	1	0.6	alone ar inte	in teach	0.6		pА
VICR	Common-mode input voltage range (see Note 5)	mperature morature		-0.2 to 2	-0.3 to 2.3	-	-0.2 to 4	-0.3 to 4.2		v
VOH	High-level output voltage	$V_{IC} = 1 V,$ $I_{OH} = -1 mA$	V _{ID} = 100 mV,	1.75	1.9	d)ov tog	3.2	3.7	104	V
VOL	Low-level output voltage	$V_{IC} = 1 V,$ $I_{OL} = 1 mA$	V _{ID} = 100 mV,		120	150		90	150	mV
AVD	Large-signal differential voltage amplification	V _{IC} = 1 V, See Note 6	R _L = 10 kΩ,	3	11		5	23	CVC 	V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V,$ R _S = 50 Ω	$V_{IC} = V_{ICR}min$,	65	78	lugil ob	65	80	VIC	dB
ksvr	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{O} = 1 V,$ $R_{S} = 50 \Omega$	V _{IC} = 1 V,	70	95		70	95	CO	dB
IDD	Supply current	V _O = 1 V, No load	V _{IC} = 1 V,		0.65	3	etar	1.4	3.2	mA

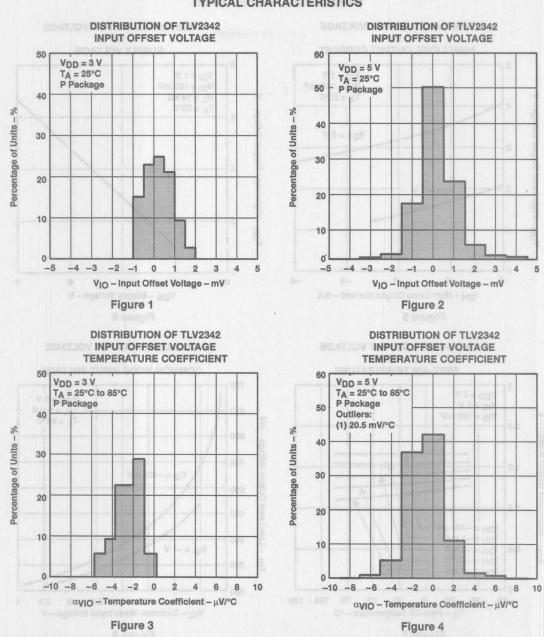
NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

ebangwiddas sa 1		
ve Frequency		
ve Supply voltage		
	va Buppy voltinge va Tempanisure va Louid objectiance va Fraquerey	Large-signal differential voltage anglification vs Froquency vs Busply voltage Phase margin vs Exercisers vs Loud objectance Equivatent Initial notes voltago

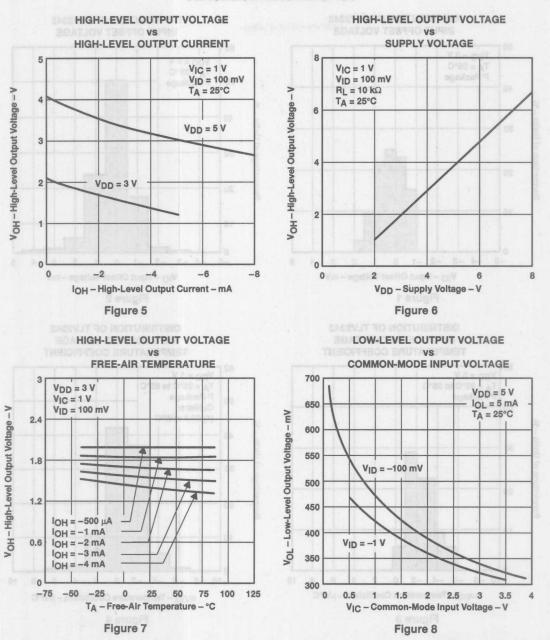


AN AYT DEEL XAX AYT NEA	· · · · · · · · · · · · · · · · · · ·	FIGURE
VIO Input offset voltage	Distribution	1,2
aVIO Input offset voltage temperature coefficient	Distribution	3, 4
	vs Output current	5
VOH High-level output voltage	vs Supply voltage	6
-0.20.30.20.0	vs Temperature	ali ebom7:ommo?
2.3 4 4.2	vs Common-mode input voltage	8
VOI Low-level output voltage	vs Temperature	9, 11
VOL Low-level output voltage	vs Differential input voltage	10
an na linas par	vs Low-level output current	12
AVD Large-signal differential voltage amplification	vs Supply voltage	13
AVD Large-signal differential voltage amplification	vs Temperature	14
IB/IO Input bias and offset currents	vs Temperature	15
VIC Common-mode input voltage	vs Supply voltage	16
Supply current	vs Supply voltage	17
DD Supply current	vs Temperature	18
SR Slew rate	vs Supply voltage	19
Sh Slew late	vs Temperature	20
VO(PP) Maximum peak-to-peak output voltage	vs Frequency	21 and 21
B1 Unity-gain bandwidth	vs Temperature	22
B ₁ Unity-gain bandwidth	vs Supply voltage	23
AVD Large-signal differential voltage amplification	vs Frequency	24, 25
	vs Supply voltage	26
om Phase margin	vs Temperature	27
	vs Load capacitance	28
Vn Equivalent input noise voltage	vs Frequency	29

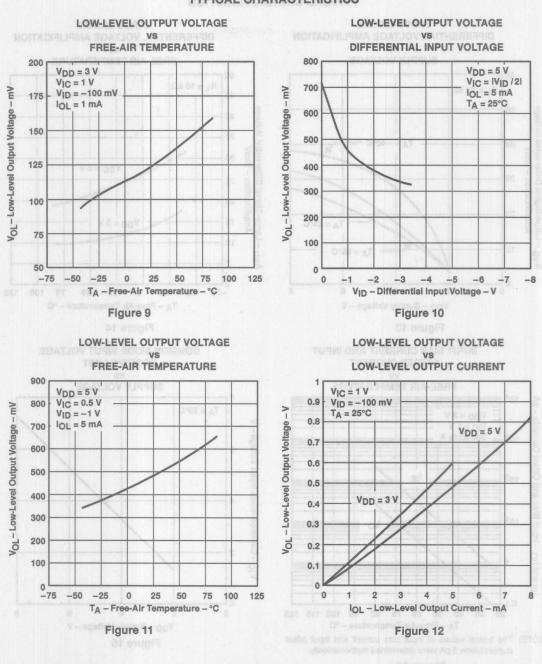




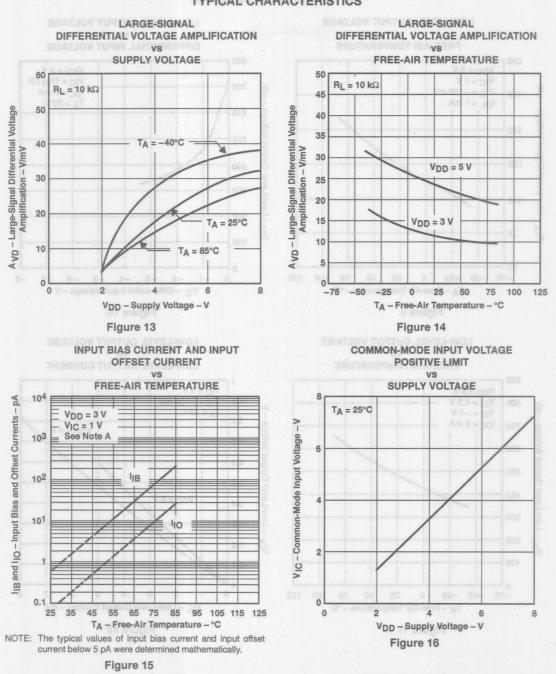


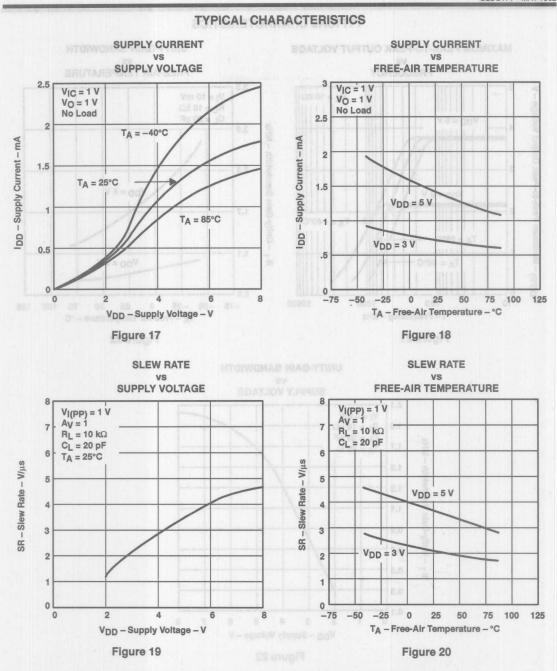




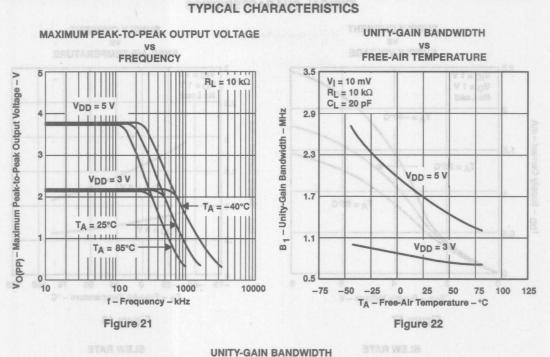












VS SUPPLY VOLTAGE 2.1 $V_1 = 3 mV$ 1.9 $R_L = 10 k\Omega$ CL = 20 pF MHZ 1.7 TA = 25°C Bandwidth -1.5 1.3 1.1 Unity-Gain 0.9 0.7 1 m 0.5 0.3 0.1 0 1 2 3 4 5 6 7 8 VDD - Supply Voltage - V Figure 23



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LinCMOS™ LOW-VOLTAGE HIGH-SPEED DUAL OPERATIONAL AMPLIFIERS SLOS114 - MAY 1992

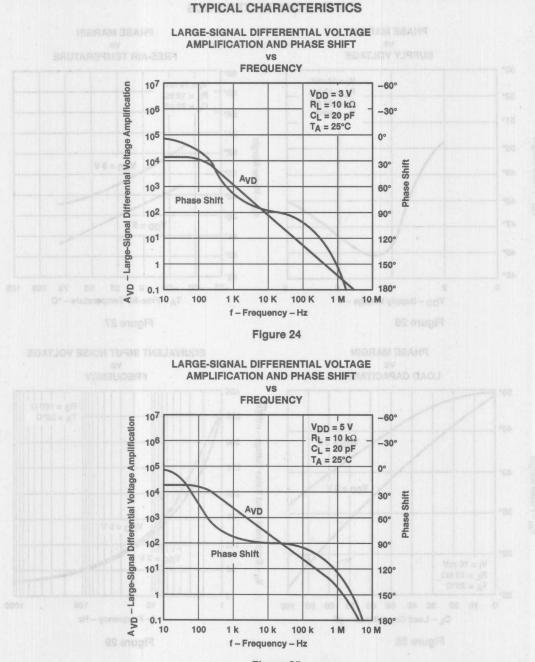
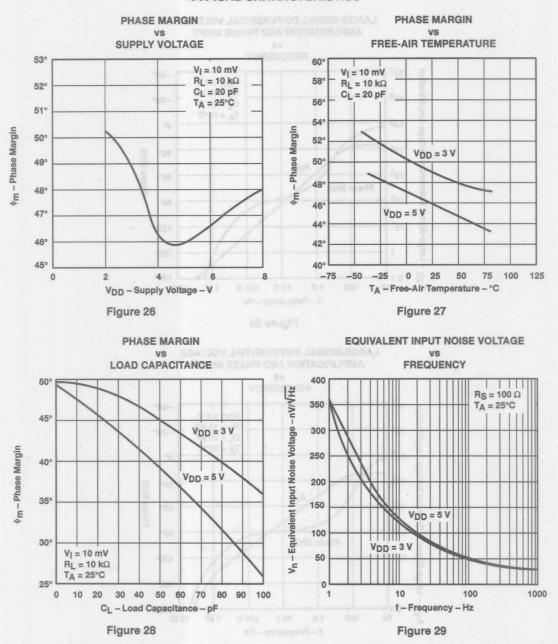


Figure 25



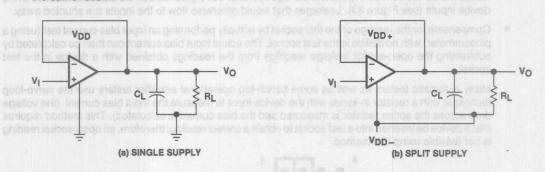


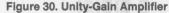


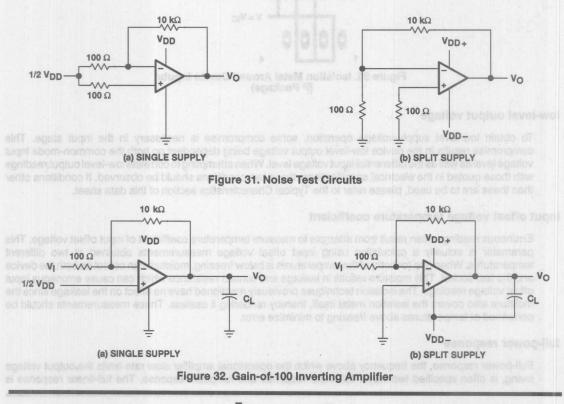
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2342 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.









TLV2342I, TLV2342Y LinCMOSTM LOW-VOLTAGE HIGH-SPEED DUAL OPERATIONAL AMPLIFIERS

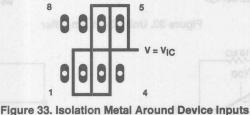
PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2342 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a
 picoammeter) with no device in the test socket. The actual input bias current can then be calculated by
 subtracting the open-socket leakage readings from the readings obtained with a device in the test
 socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.



(P Package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

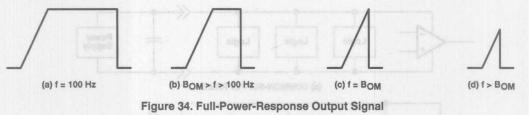
Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is



PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2342 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to V_{DD}/2, while consuming very little power and is suitable for supply voltages of greater than 4 V.

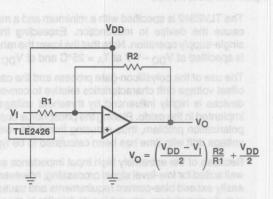


Figure 35. Inverting Amplifier With Voltage Reference



APPLICATION INFORMATION

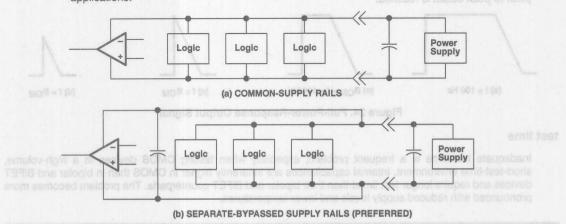
single-supply operation (continued)

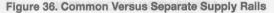
The TLV2342 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

 Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.

Preintal

Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.





input characteristics

The TLV2342 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower the range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

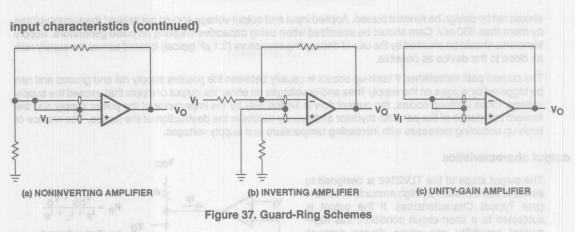
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2342 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2342 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



APPLICATION INFORMATION



noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2342 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

electrostatic-discharge protection

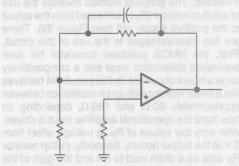


Figure 38. Compensation for Input Capacitance

The TLV2342 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2342 inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes



APPLICATION INFORMATION

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2342 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this highcurrent capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2342 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60Ω and 180Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

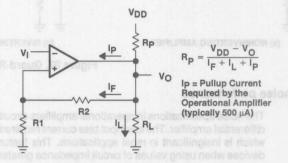


Figure 39. Resistive Pullup to Increase VOH

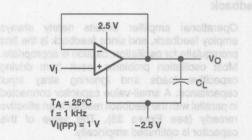


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2342 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

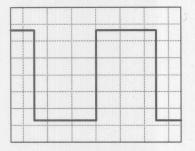
su-dola

Recause CMOS devices are susceptible to intoll-up due to their horent parentition tryviators, the TLV2342 inputs and outputs are designed to withstand – 100 mA surge surrents without sustaining latch-up; however, extrainings should be used to reduce the charge of subt-up whenever opening, internal protection diodes

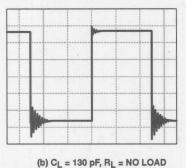


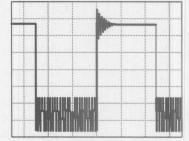
APPLICATION INFORMATION

output characteristics (continued)



(a) $C_L = 20 \text{ pF}$, $R_L = \text{NO LOAD}$





(c) $C_L = 150 \text{ pF}$, $R_L = \text{NO LOAD}$

Figure 41. Effect of Capacitive Loads

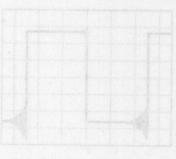


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And the second second



(a) G. + 150 pr. R. + NO LOAD

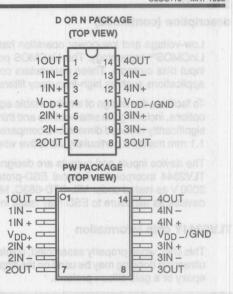
Nouro 41. Effect of Capacitive Lond:

- Wide Range of Supply Voltages Over Specified Temperature Range: -40°C to 85°C...2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rall and up to V_{DD} –1 V at 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance ... 10¹² Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

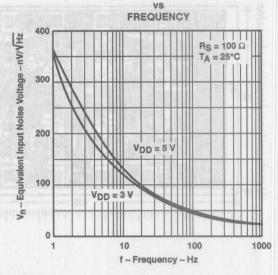
description

The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2344 is designed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2344 has a typical slew rate of 2.1 V/µs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of -40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.



EQUIVALENT INPUT NOISE VOLTAGE



AVAILABLE OPTIONS

	Viemov	PAC	CKAGED DEVICE	IS	
TA	VIOmax AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	CHIP FORM (Y)
-40°C to 85°C	10 mV	TLV2344ID	TLV2344IN	TLV2344IPWLE	TLV2344Y

UMENTS

POST OFFICE BOX 655303 @ DALLAS, TEXAS 75265

Available in tape and reel. Add R suffix to the device type when ordering (e.g., TLV2344IDR). The PW package is only available left-end taped and reeled (e.g., TLV2344IPWLE).

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PRODUCTION DATA Information is current as of publication data. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters. Copyright © 1992, Texas Instruments Incorporated

2-233

description (continued)

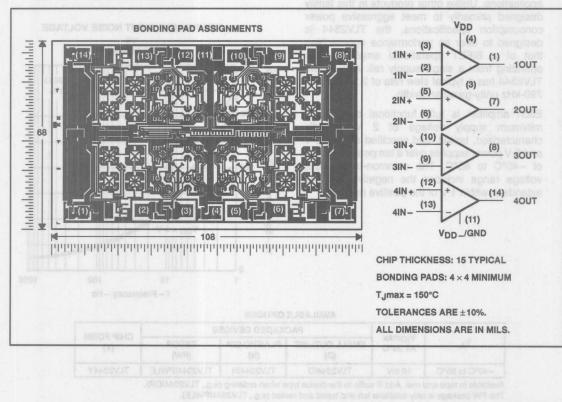
Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2344 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

To facilitate the design of small portable equipment, the TLV2344 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2344 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

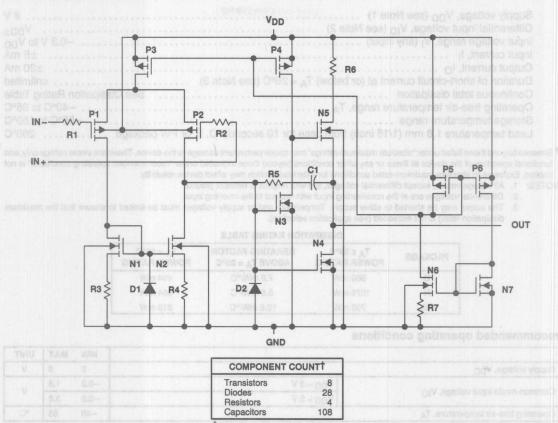
TLV2344Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2344I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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equivalent schematic (each amplifier)



[†] Includes both amplifiers and all ESD, bias, and trim circuitry



TLV2344I LinCMOSTM LOW-VOLTAGE HIGH-SPEED QUAD OPERATIONAL AMPLIFIER SLOS115 - MAY 1992

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V _{DD} (see Note 1) 8 V Differential input voltage, V _{ID} (see Note 2) V _{DD±} Input voltage range, V _I (any input) -0.3 V to V _{DD}	
Input current, II ±5 mA	
Output current, IO	
Duration of short-circuit current at (or below) T _A = 25°C (see Note 3) unlimited	
Continuous total dissipation	
Operating free-air temperature range, T _A 40°C to 85°C	
Storage temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package 260°C	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application selection).

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE TA = 25°C	T _A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1575 mW	5.6 mW/°C	364 mW
PW	700 mW	12.6 mW/°C	819 mW

recommended operating conditions

	printer a series of the series	MIN	MAX	UNIT
Supply voltage, VDD	COMPONENT COUNTY	2	8	V
	V _{DD} = 3 V motelanet T	-0.2	1.8	N
Common-mode input voltage, VIC	$V_{DD} = 5 V$	-0.2	3.8	V
Operating free-air temperature, TA	Capacitam 108	-40	85	°C

when him and the sold the



	LINESV.T					TLV2	3441			
	PARAMETER	TEST CONDITIONS	TAT	V	DD = 3 \	/	۷	DD = 5 V	1	UNIT
		s Nt = iden	VE	MIN	TYP	MAX	MIN	TYP	MAX	
Vio	Input offset voltage	$V_{O} = 1 V$, $V_{IC} = 1 V$, $R_{S} = 50 \Omega$,	25°C	81 = \$4082	1.1	10	akig yi	1.1	10	mV
.10		$R_L = 10 k\Omega$	Full range	11-11		12		unit front	12	
αNIO	Average temperature coefficient of input offset voltage	S	25°C to 85°C	See F	2.7			2.7		μV/°C
lio	Input offset current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	- 16.	0.1	10/10/2012/201	Beiling	0.1		Aq
10	input onset current (see Note 4)	vO = 1 v, $vIC = 1 v$	85°C	L.N.	22	1000		24	1000	рА
IIB	Input bias current (see Note 4)	$V_{O} = 1 V$, $V_{IC} = 1 V$	25°C	R	0.6		TOOLAS	0.6	S-QINO	pA
D		10-11, 10-11	85°C	t with	175	2000		200	2000	pri
	Common-mode input	ي + 10 kcs2 6	25°C	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		v
VICR	voltage range (see Note 5)	erature, V _{DD} = 3	Full range	-0.2 to 1.8	allios	38 <u>86</u> 8	-0.2 to 3.8	araote	ng ch	v
11012	XAM SYT MM	V _{IC} = 1 V,	25°C	1.75	1.9		3.2	3.7		
Vон	High-level output voltage	V _{ID} = 100 mV, I _{OH} = -1 mA	Full range	1.7			3			V
an//A	8.9	V _{IC} = 1 V,	25°C	- 10	120	150	Trisp vi	90	150	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 1 \text{ mA}$	Full range	1.086		190			190	mV
SHWW	Large-signal differential	$V_{IC} = 1 V,$	25°C	3	11	egalia	5	23	Equivas	
AVD	voltage amplification	$R_L = 10 k\Omega$, See Note 6	Full range	2			3.5			.V/MV
OMDD		$V_{O} = 1 V$,	25°C	65	78		65	80		10
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min,$ R _S = 50 Ω	Full range	60			60	ein bend	Unity-9	dB
ksvr	Supply-voltage rejection ratio	$V_{IC} = 1 V$, $V_{O} = 1 V$,	25°C	70	95		70	95		dB
SVR	(ΔV _{DD} /ΔVIO)	Rs = 50 Ω	Full range	65			65	nipism	Phate	aB
	Supply current	$V_{O} = 1 V$, $V_{IC} = 1 V$,	25°C	A see	1.3	6		2.7	6.4	mA
DD	Supply current	No load	Full range			8			8.8	mA

¹ Full range is -40°C to 85°C.
NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.



TLV2344I, TLV2344Y LinCMOSTM LOW-VOLTAGE HIGH-SPEED QUAD OPERATIONAL AMPLIFIERS SLOS115 - MAY 1992

	DADAMETED	TERTO	TEST CONDITIONS		TLV2344I	LIMIT
	PARAMETER	TESTO	ONDITIONS	TA	MIN TYP MAX	UNIT
0.0	XAM SYT MM XAM SYT	VIC = 1 V,	$V_{I(PP)} = 1 V,$	25°C	2.1	Nue
SR	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$, See Figure 30	CL = 20 pF,	85°C 1.7		V/µs
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	25	nV/√Hz
D.		Vo = VoH,	CL = 20 pF,	25°C	170	Lul-
BOM	Maximum output swing bandwidth	$R_L = 10 k\Omega$,	See Figure 30	85°C	145	kHz
	22 1 600 AS	V _I = 10 mV,	$C_{1} = 20 \text{ pF},$	25°C	790	Let la
B ₁	Unity-gain bandwidth	R _L = 10 kΩ,	See Figure 32	85°C	690	kHz
	2000 2000 2000	$V_{I} = 10 \text{ mV},$	f = B ₁ ,	-40°C	53°	
φm	Phase margin	CL = 20 pF,	R _L = 10 kΩ,	25°C	49°	1
		See Figure 32		85°C	47°	1

operating characteristics at specified free-air temperature, V_{DD} = 5 V

	DADAMETER	TEOTO		-	TLV2344I	
	PARAMETER	TESTO	ONDITIONS	TA	MIN TYP MAX	UNIT
(N)	The second s	VIC = 1 V,	N	25°C	3.6	HQ.
0.0	Olaw ante at units ania	$R_{l} = 10 \text{ k}\Omega,$	VI(PP) = 1 V	85°C	2.8	Nue
SR	Slew rate at unity gain	CL = 20 pF,	N	25°C	2.9	V/µs
		See Figure 30	VI(PP) = 2.5 V	85°C	2.3	10
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R _S = 100 Ω,	25°C	25	nV/√Hz
	8.8	Vo = VoH,	$C_1 = 20 \text{pF},$	25°C	320	i.u.
BOM	Maximum output swing bandwidth	$R_L = 10 k\Omega$,	See Figure 30	85°C	250	kHz
68	11-1	V _I = 10 mV,	$C_1 = 20 \text{pF},$	25°C	1.7	FURM
B ₁	Unity-gain bandwidth	RL = 10 kΩ,	See Figure 32	85°C	1.2	MHz
- ch	25 70 95	VI = 10 mV,	f = B ₁ ,	-40°C	49°	RVA
φm	Phase margin	CL = 20 pF,	R _L = 10 kΩ,	25°C	46°	1.1.1.
		See Figure 32		85°C	43°	

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12.0 - r.V. V.S. - r.r.V is V.S. of V.S. 0 - r.V. V.S. - r.S.V.



					TLV2	344Y			
	PARAMETER	TEST CONDITIONS	V	DD = 3	V	V	DD = 5 \	/	UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	$V_{O} = 1 V, V_{IC} = 1 V,$ R _S = 50 Ω, R _L = 10 kΩ		1.1	10) offsnit w	1.1	10	mV
IIO	Input offset current (see Note 4)	$V_{O} = 1 V, V_{IC} = 1 V$		0.1	1		0.1		pА
IIB	Input bias current (see Note 4)	V _O = 1 V, V _{IC} = 1 V		0.6	and so the second	trend out	0.6	in the	рА
VICR	Common-mode input voltage range (see Note 5)	va Terriporature va Connesio-moda inj	-0.2 to 2	-0.3 to 2.3		-0.2 to 4	-0.3 to 4.2		V
VOH	High-level output voltage	$V_{IC} = 1 V$, $V_{ID} = 100 mV$, $I_{OH} = -1 mA$	1.75	1.9	salicy tuc	3.2	3.7	VOL	V
VOL	Low-level output voltage	$V_{IC} = 1 V$, $V_{ID} = -100 mV$, $I_{OL} = 1 mA$		120	150		90	150	mV
AVD	Large-signal differential voltage amplification	$V_{IC} = 1 V$, $R_L = 10 k\Omega$, See Note 6	3	11	in the Real	5	23	aver.	V/mV
CMRR	Common-mode rejection ratio	$V_{O} = 1 V, V_{IC} = V_{ICR}$ min, R _S = 50 Ω	65	78	r tulgri el	65	80	OIV.	dB
k SVR	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{ID})$	$V_{O} = 1 V, \qquad V_{IC} = 1 V, \\ R_{S} = 50 \Omega$	70	95	3	70	95	001	dB
IDD	Supply current	$V_O = 1 V, V_{IC} = 1 V,$ No load		1.3	6	elst	2.7	6.4	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically. 5. This range also applies to each input individually. 6. At $V_{PD} = 5 V_{PD} = 0.25 V_{PD} = 3.2 V_{PD} = 0.5 V_{PD} = 0.5 V_{PD}$

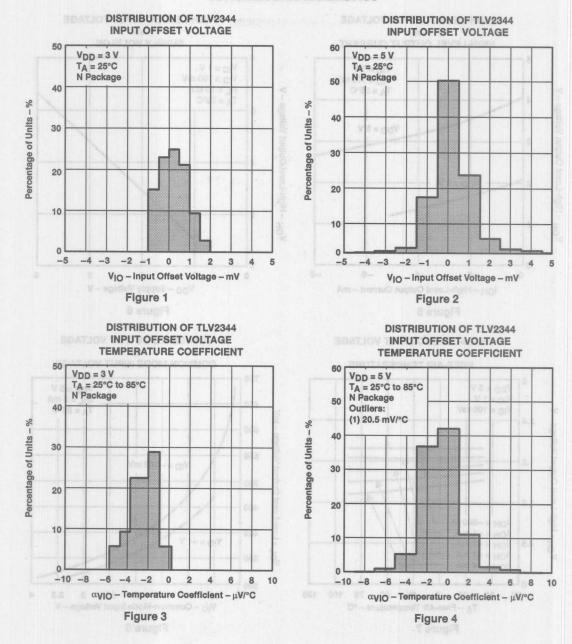


KAN AVT MM I KAN AVT HIM			FIGURE
VIO Input offset voltage		Distribution	1,2
aVIO Input offset voltage temperature coefficie	ent	Distribution	3, 4
and the second		vs Output current	5
VOH High-level output voltage		vs Supply voltage	6
Low-level output voltage	No.	vs Temperature	7
2.8 4 4.2		vs Common-mode input voltage	8
	Men OOt	vs Temperature	9, 11
VOL Low-level output voltage		vs Differential input voltage	10
and the second	Vm cot-s	vs Low-level output current	12
AVD Large-signal differential voltage amplifica	ation	vs Supply voltage	13
IO Input bias and offset currents	auon	vs Temperature	14
IIB/IIO Input bias and offset currents		vs Temperature	15
VIC Common-mode input voltage	1.	vs Supply voltage	16
la Supply ourrest		vs Supply voltage	17
IDD Supply current	N.L.	vs Temperature	18
SR Slew rate		vs Supply voltage	19
SH Slew fate		vs Temperature	20
VO(PP) Maximum peak-to-peak output voltage	lad Premuo.	vs Frequency	21
D Units and the sector faile		vs Temperature	22
B1 Unity-gain bandwidth	0.5 V to 1.5	vs Supply voltage	23
AVD Large-signal differential voltage amplifica	ation	vs Frequency	24, 25
		vs Supply voltage	26
φm Phase margin		vs Temperature	27
		vs Load capacitance	28
Vn Equivalent input noise voltage		vs Frequency	29
Phase shift		vs Frequency	24, 25

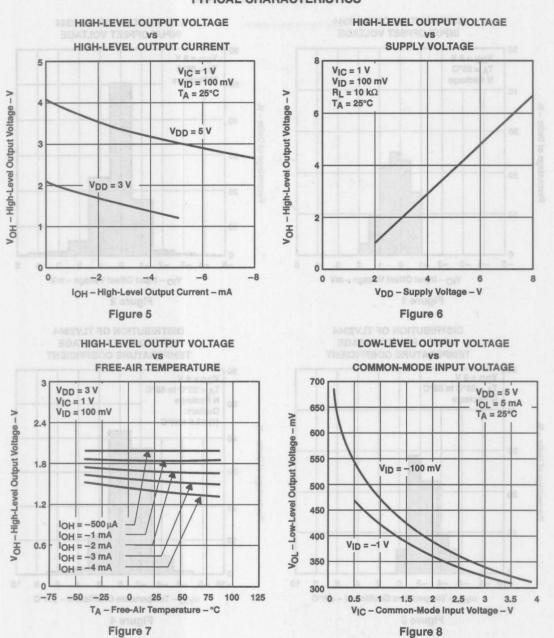
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

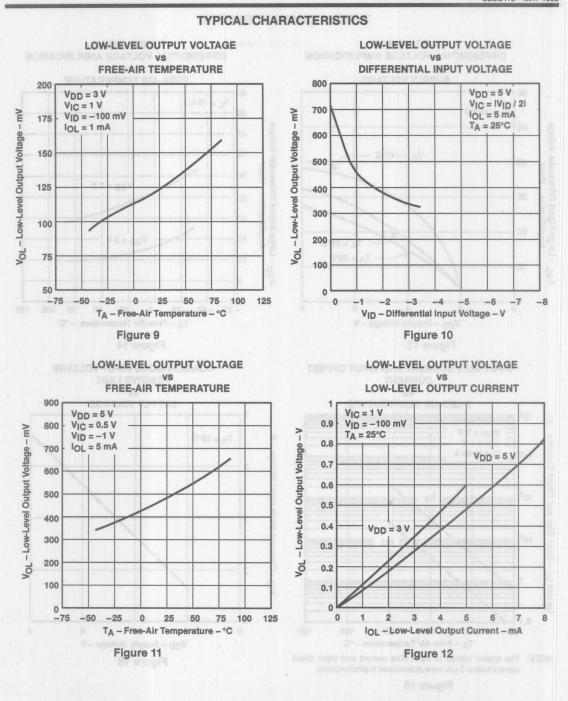




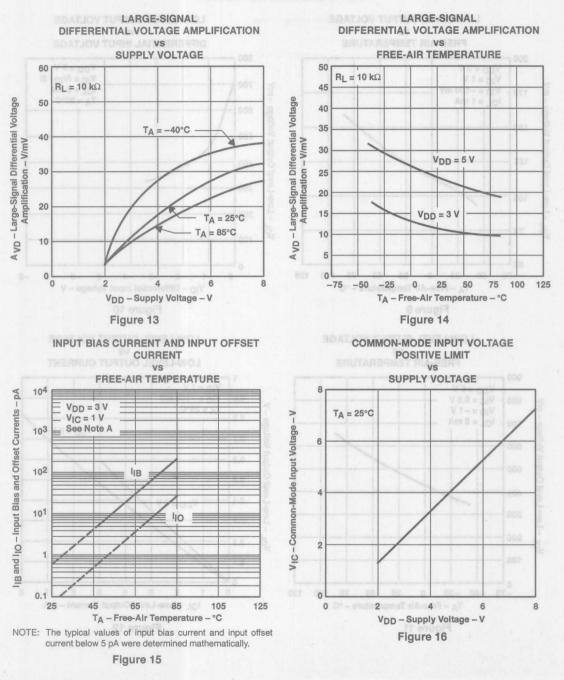


TYPICAL CHARACTERISTICS





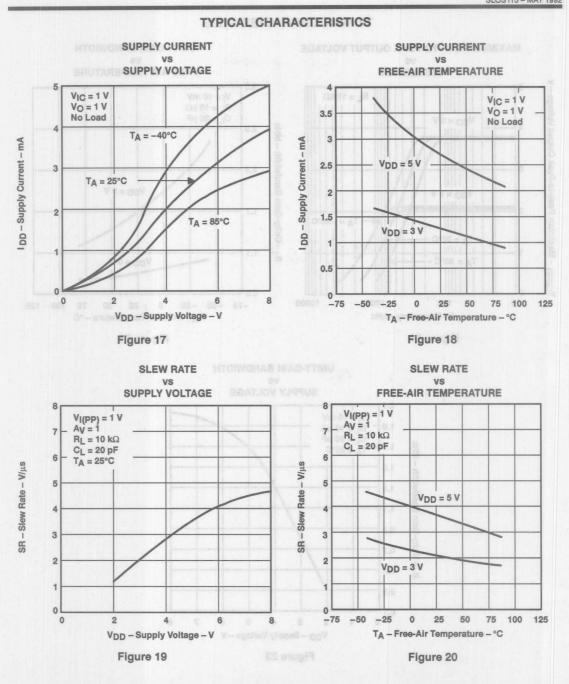




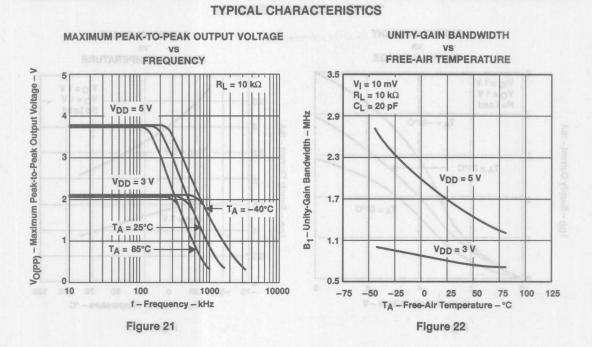
IEXAS INSTRUMENTS

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TYPICAL CHARACTERISTICS







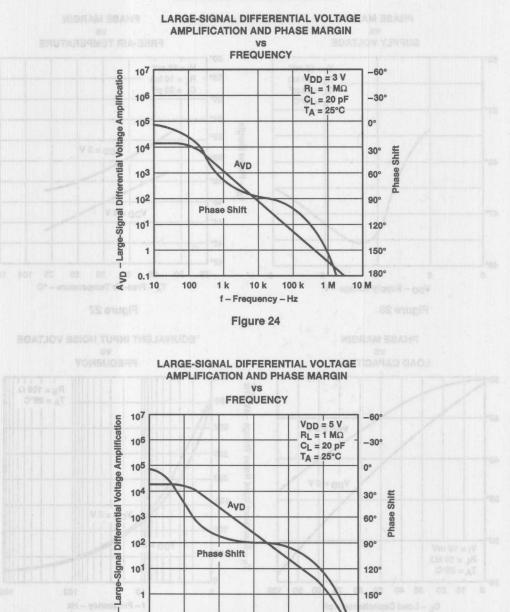
UNITY-GAIN BANDWIDTH VS SUPPLY VOLTAGE 2.1 $V_I = 10 \text{ mV}$ 1.9 $R_L = 10 k\Omega$ CL = 20 pF 1.7 Unity-Gain Bandwidth – MHz TA = 25°C 1.5 1.3 1.1 0.9 0.7 B1-0.5 0.3 0.1 0 1 2 3 4 5 6 7 8 VDD - Supply Voltage - V Figure 23

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180°

10 M

TYPICAL CHARACTERISTICS



10 k

f – Frequency – Hz Figure 25

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100 k

1 M

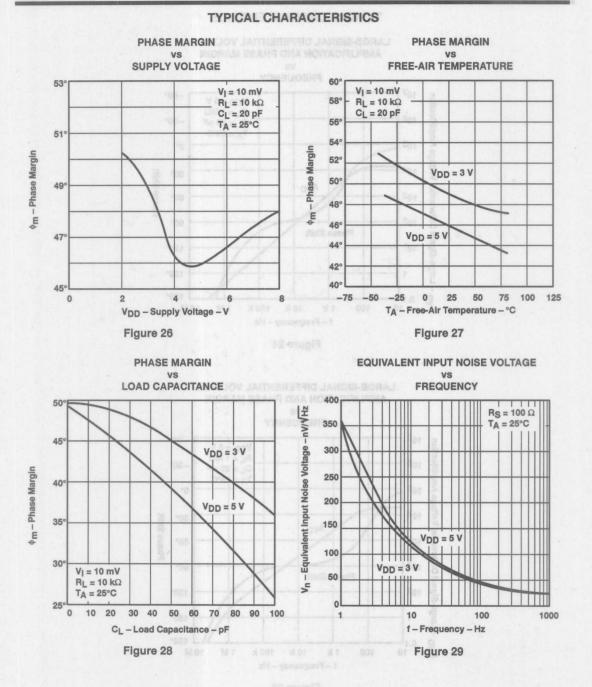
AVD

0.1

10

100

1 k



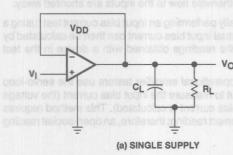
XAS UMENTS

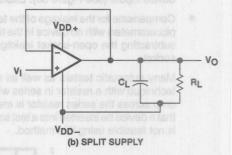
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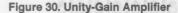
PARAMETER MEASUREMENT INFORMATION

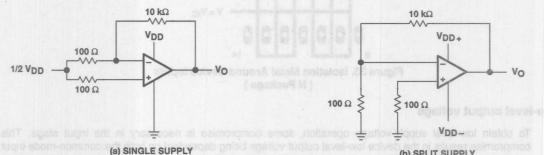
single-supply versus split-supply test circuits

Because the TLV2344 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



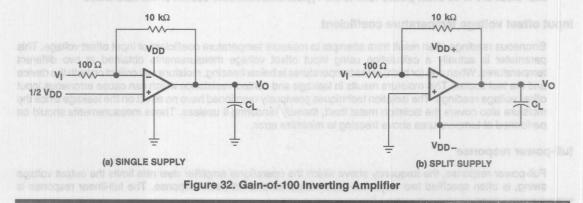






(b) SPLIT SUPPLY

Figure 31. Noise Test Circuit





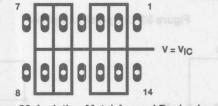
PARAMETER MEASUREMENT INFORMATION

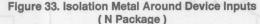
input bias current

Because of the high input impedance of the TLV2344 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.





low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is



PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2344 performs well using dualpower supplies (also called balanced or split supplies), the design is optimized for singlesupply operation. This includes an input commonmode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to V_{DD}/2 while consuming very little power and is suitable for supply voltages of greater than 4 V.

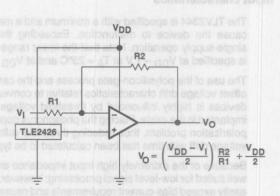


Figure 35. Inverting Amplifier With Voltage Reference

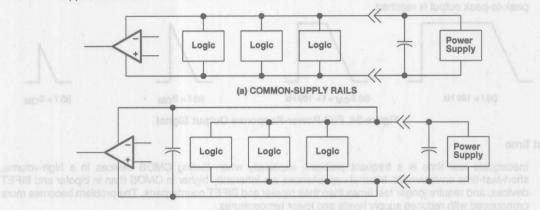


APPLICATION INFORMATION

single-supply operation (continued)

The TLV2344 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(b) SEPARATE-BYPASSED SUPPLY RAILS (PREFERRED)



input characteristics

The TLV2344 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25^{\circ}$ C and at $V_{DD} - 1.2$ V at all other temperatures.

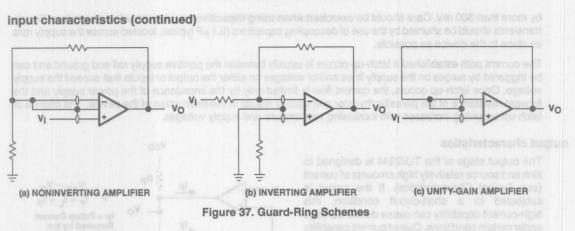
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2344 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2344 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



APPLICATION INFORMATION

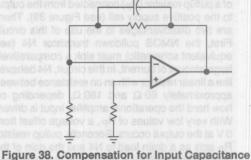


noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2344 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

feedback

Operational amplifiers circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.



electrostatic-discharge protection

The TLV2344 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C. Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2344 inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage



APPLICATION INFORMATION

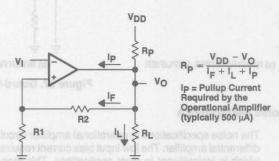
by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2344 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2344 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.





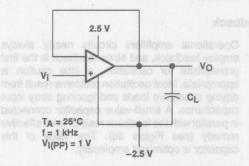


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2344 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

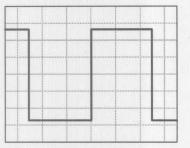
0.8-11078

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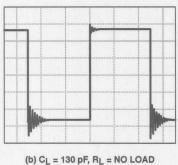


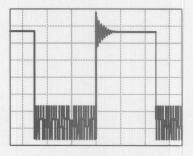
TYPICAL APPLICATION DATA

output characteristics (continued)



(a) CL = 20 pF, RL = NO LOAD





(c) CL = 150 pF, RL = NO LOAD

Figure 41. Effect of Capacitive Loads



TLV2344I, TLV2344I, InCMOST* LOW-VOLTAGE HICH-SPEED QUAD OPERATIONAL AMPLIFIERS

TYPICAL APPLICATION DATA

output characteristics (continued



(c) (c) = 160 (c), R_ = NO LOAI

- (0) OF 4 190 PR - 10 CM - 10 (0)

D OR P PACKAGE

7 20UT

8 VCC+

8 VCC+

7 20UT

6 21N-

5 2IN+

6 2IN-

5 1 2IN+

(TOP VIEW)

PW PACKAGE

(TOP VIEW)

10UT

1IN-[2

1IN+[] 3

1

Vcc-[

10UT 10

1IN- 00 2

1IN+ 0 3

Vcc-

- Low Supply Voltage Operation
 V_{CC} = ± 1 V Min
- Wide Output Voltage Swing ±2.4 V Typ at V_{CC±} = ±2.5 V, R_L = 10 kΩ
- Wide Bandwidth 7 MHz Typ at V_{CC±} = 2.5 V
- Low Noise ... 8 nV/√Hz Typ at f = 1 kHz
- High Slew Rate 4 V/µsec Typ at V_{CC+} = ±2.5 V
- Available In Small TSSOP Packages

description

The TLV2362I is a high-performance dual operational amplifier built using an original Texas Instruments bipolar process. This device can be

operated at a very low supply voltage $(\pm 1 \text{ V})$, while maintaining a wide output swing. The TLV2362I offers a dramatically improved dynamic range of signal conditioning in low-voltage systems. Coupled with this high performance, the TLV2362I provides a wider unity-gain bandwidth and higher slew rate than other general-purpose operational amplifiers. With its low distortion and low noise performance, this device is well suited for audio applications. The TLV2362I is available in the thin-shrink small-outline package (TSSOP) to reduce board space requirements.

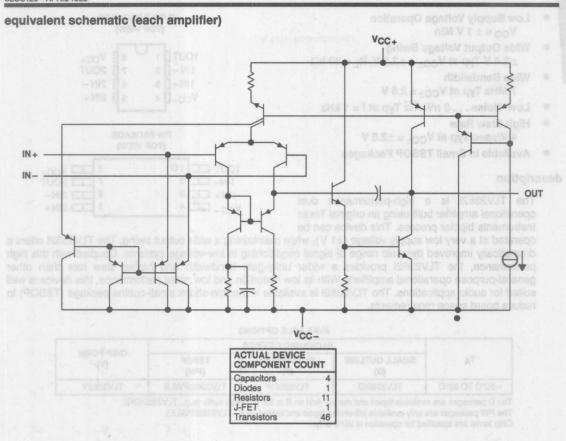
AVAILABLE OPTIONS

		PACKAGED DEVICES	3	
Τ _A	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
-20°C TO 85°C	TLV2362ID	TLV2362IP	TLV2362IPWLE	TLV2362Y

The D packages are available taped and reeled. Add an R to the package suffix (e.g., TLV2362IDR). The PW packages are only available left-ended taped and reeled, (e.g., TLV2362IPWLE). Chip forms are specified for operation at 25°C only.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include teeting of all parameters.

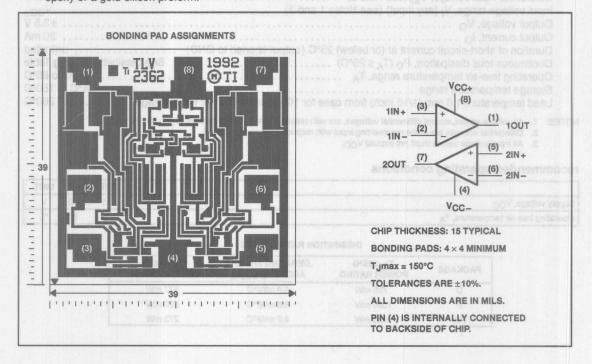




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TLV2362Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2362I. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC+} (see Note 1) 3.5 V
Supply voltage, V _{CC} - (see Note 1)
Differential input voltage, VID (see Note 2)
Input voltage range, V _I (any input) (see Notes 1 and 3) V _{CC+}
Output voltage, V _O ±3.5 V
Output current, Io
Duration of short-circuit current at (or below) 25°C (output shorted to GND) unlimited
Continuous total dissipation, $P_D(T_A \le 25^{\circ}C)$
Operating free-air temperature range, T _A
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} . 2. Differential voltages are at the noninverting input with respect to the inverting input.

- 3. All input voltage values must not exceed VCC.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V _{CC}	±1	±2.5	V
Operating free-air temperature, TA	-20	85	°C

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	T _A ≤ 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
PARMO	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW



	TLYESON		TA	٦	LV2362		
	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	265	2985			1	6	mV
VIO	Input offset voltage	$V_{O} = 0, \qquad V_{IC} = 0$	-20°C to 85°C		ander no can	7.5	mv
	Input offset current	No 0 Nio 0	25°C		5	100	nA
10	Input onset current	V _O = 0, V _{IC} = 0 -	-20°C to 85°C			150	TIA
lue.	Input bios surrent	No. 0 Vio. 0	25°C		20	150	nA
IB	Input bias current	$V_{O} = 0, \qquad V_{IC} = 0$	-20°C to 85°C		CT ICR/ SON	250	IIA
	25 *0 ** ±1.5	IV _{IO} I ≤ 7.5 mV	25 °C	±0.5			
VICR	Common-mode input voltage		-20°C to 85°C	±0.5			V
Varia	25%0 2 2.4	$R_L = 10 k\Omega$	25°C	1.2	1.4		v
VOM+	Maximum positive-peak output voltage	$R_L \ge 10 \ k\Omega$	-20°C to 85°C	1.2			V
Vau	NS	$R_L = 10 \text{ k}\Omega$	25°C	-1.2	-1.4	Maxim	v
VOM-	Maximum negative-peak output voltage	$R_L \ge 10 \ k\Omega$	-20°C to 85°C	-1.2			V
Act	Sumply summer (both smallfiers)	No. No.	25°C	mus ellesel	2.8	4.5	'nA
ICC	Supply current (both amplifiers)	$V_{O} = 0$, No load	-20°C to 85°C	and the second s		5.5	Am [
AVD	Large-signal differential voltage amplification	$V_O = \pm 1 V$, $R_L = 10 k\Omega$	25°C	SAMENT	55	egnal	dB
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 0.5 V$	25°C	KORT BUILT	75	Condia	dB
ksvr	Supply-voltage rejection ratio	$V_{CC+} = \pm 1.5 \text{ V to } \pm 2.5 \text{ V}$	25°C	nodosjek	80	Midding .	dB

operating characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C

PARAMETER		also movioo ma	TEST CONDITION		and the second second	LV2362	1	LINUT
			TEST CONDITIONS			TYP	MAX	UNIT
SR	Slew rate	Ay = 1,	VI = ±0.5 V	Contraction of the second second		2.5	6(6) 10	V/µs
B ₁	Unity-gain bandwidth	Ay = 40,	RL = 10 kΩ,	CL = 100 pF	(313	6	ning-yn	MHz
Vn	Equivalent input noise voltage	R _S = 20 Ω,	$R_F = 2 k\Omega$,	f = 1 kHz	itilav ittir	9	Indexin	nV/√Hz



-	TLYBORN	TEAT COMPLETIONS	-	TLV2362I			
	PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
	8 0%85	N= 0 N= 0	25°C		1	6	
VIO	Input offset voltage	$V_{O} = 0, \qquad V_{IC} = 0$	-20°C to 85°C			7.5	mV
in her	logit affect oursent	Vo 0 Vic 0	25°C		5	100	nA
10	Input offset current	$V_{O} = 0, \qquad V_{IC} = 0$	-20°C to 85°C			150	nA C
	Input bias current	$V_{O} = 0$, $V_{IC} = 0$	25°C		20	150	nA
IB	input bias current	$V_{O} = 0, \qquad V_{IC} = 0$	-20°C to 85°C			250	IIA
	Common-mode input voltage	IV _{IO} I ≤ 7.5 mV	25 °C	±1.5			V
VICR	Common-mode input voltage	10 01 2 1.3 1110	-20°C to 85°C	±1.4	proju-ur	anjimot.	YO
	AN S.T. OTES	RL = 10 kΩ	25°C	2	2.4		V
VOM+	Maximum positive-peak output voltage	R _L ≥ 10 kΩ	-20°C to 85°C	2	in positi	Madre	V
Vau	AI	R _L = 10 kΩ	25°C	-2	-2.4		V
VOM-	Maximum negative-peak output voltage	R _L ≥ 10 kΩ	-20°C to 85°C	-2		Maxim	Vio
	Supply current (both amplifiers)	V- 0 Nolord	25°C		3.5	5	
ICC	Supply current (both amplifiers)	$V_{O} = 0$, No load	-20°C to 85°C	ana man (aan an a		6	mA
AVD	Large-signal differential voltage amplification	$V_O = \pm 1 V$, $R_L = 10 k\Omega$	25°C	Inithese	60	-onie L	dB
CMRR	Common-mode rejection ratio	V _{IC} = ± 0.5 V	25°C	nitonia	85	Commo	dB
KSVR	Supply-voltage rejection ratio	$V_{CC+} = \pm 1.5 V \text{ to } \pm 2.5 V$	25°C	- Sthele	80	Same	dB

electrical characteristics, $V_{CC+} = \pm 2.5 V$ (unless otherwise noted)

operating characteristics, $V_{CC\pm} = \pm 2.5 \text{ V}$, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS			TLV23621			UNIT
		SPE CONDUMNAS	MIN	TYP	MAX	UNIT		
SR	Slew rate	A _V = 1, V _I = ±0.5 V			3		alerwa	V/µs
B ₁	Unity-gain bandwidth	Av = 40,	R _L = 10 kΩ,	CL = 100 pF	-10	7	nino-eni	MHz
Vn	Equivalent input noise voltage	R _S = 20 Ω,	$R_F = 2 k\Omega$,	f = 1 kHz	niov and	8	frontziolen	nV/√Hz



	DADAMETER	TEST C	Т	1	UNIT		
	PARAMETER	TEST C	MIN	TYP	MAX	UNIT	
VIO	Input offset voltage	V _O = 0,	$V_{IC} = 0$		1	6	mV
IIO	Input offset current	V _O = 0,	VIC = 0		5	100	nA
IIB	Input bias current	V _O = 0,	$V_{IC} = 0$		20	150	nA
VICR	Common-mode input voltage	$ V_{IO} \le 7.5 \text{ m}$	/	±0.5			V
VOM+	Maximum positive-peak output voltage	R _L = 10 kΩ		1.2	1.4		v
VOM-	Maximum negative-peak output voltage	R _L = 10 kΩ		-1.2	-1.4		v
ICC	Supply current (both amplifiers)	V _O = 0,	No load		2.8	4.5	mA
AVD	Large-signal differential voltage amplification	$V_{O} = \pm 1 V$,	RL = 10 kΩ		55		dB
CMRR	Common-mode rejection ratio	VIC = ± 0.5 V			75	1	dB
ksvr	Supply-voltage rejection ratio	$V_{CC\pm} = \pm 1.5$	V to ± 2.5 V		80		dB

electrical characteristics, $V_{CC+} = \pm 1.5 V$, $T_A = 25^{\circ}C$ (unless otherwise noted)

operating characteristics, V_{CC \pm} = ±1.5 V, T_A = 25°C

PARAMETER		TEAT COMPLETIONS	1	TLV2362Y		
		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	$A_V = 1$, $V_I = \pm 0.5 V$		2.5		V/µs
B ₁	Unity-gain bandwidth	$A_V = 40$, $R_L = 10 k\Omega$, $C_L = 100$	pF	6		MHz
Vn	Equivalent input noise voltage	$R_S = 20 \Omega$, $R_F = 2 k\Omega$, $f = 1 kHz$		9		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ± 2.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEOTO	TEST CONDITIONS		TLV2362Y			
		TESTO			TYP	MAX	UNIT	
VIO	Input offset voltage	V _O = 0,	$V_{IC} = 0$		1	6	mV	
10	Input offset current	V _O = 0,	$V_{IC} = 0$		5	100	nA	
IB .	Input bias current	V _O = 0,	$V_{IC} = 0$		20	150	nA	
VICR	Common-mode input voltage	IV _{IO} I ≤ 7.5 m	V	±1.5			V	
VOM+	Maximum positive-peak output voltage	R _L = 10 kΩ		2	2.4		V	
VOM-	Maximum negative-peak output voltage	R _L = 10 kΩ		-2	-2.4		V	
ICC	Supply current (both amplifiers)	V _O = 0,	No load		3.5	5	mA	
AVD	Large-signal differential voltage amplification	$V_{O} = \pm 1 V$,	RL = 10 kΩ		60		dB	
CMRR	Common-mode rejection ratio	V _{IC} = ± 0.5 V			85		dB	
k SVR	Supply-voltage rejection ratio	$V_{CC\pm} = \pm 1.5$	V to ± 2.5 V		80		dB	

operating characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS		TLV2362Y			UNIT
PARAMETER		TEST CONDITIONS			TYP	MAX	
SR	Slew rate	$A_V = 1$, $V_I = \pm 0.5 V$			3		V/µs
B ₁	Unity-gain bandwidth	Ay = 40, RL = 10 kΩ, CL =	= 100 pF		7		MHz
Vn	Equivalent input noise voltage	$R_{S} = 20 \Omega$, $R_{F} = 2 k\Omega$, $f = 1$	kHz		8		nV/√Hz



DUAL HIGH-PERFORMANCE, LOW-VOLTAGE OPERATIONAL AMPLIFIERS

stectrical characteristics, Vcc+ = ±1.5 V, TA = 25°C (unloss of)crivitae noted)

	VIOLES				

operating characterizatics, Voor+ = ±1.5 V, TA = 25°C

	Av = 40, BL = 10 kg, CL = 100 pF	
0		

electrical characteristics, Vnns = ±2.5 V, Ta = 25°C (unless otherwise noted)

			TEAT CONDITIONS				
			Vic +0				

operating obstactoristics, $V_{CC+} = \pm 2.5 V$, $T_{A} = 25^{\circ}C$



General Information	1	
Operational Amplifiers	2	
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	General Information
	Operational Amplifiers
	Comparators
	Voltage Regulators
	P-Channel MOSFETs
8	Analog-to-Digital Converters
	Line Driver/Receiver
	Mechanical Data

SLCS121 - AUGUST 1993 Low-Voltage and Single-Supply Operation D OR P PACKAGE (TOP VIEW) $V_{CC} = 2 V to 7 V$ **Common-Mode Voltage Range That** 10UT 8 Vcc **Includes** Ground 7 20UT 1IN-I 2 **Fast Response Time** 1IN+ 3 6 2IN-450 ns Typ (TLV2393) GNDI 4 5 2IN+ Low Supply Current **PW PACKAGE** 0.7 mA Typ (TLV1393) (TOP VIEW) Specified Fully at 3-V and 5-V Supply Voltages 8 VDD+ 10UT 10 1IN- 0 2 7 **20UT** 1IN+ 🖂 3 6 21N-GND C 4 5 2IN+

description

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The TLV1393 and the TLV2393 are dual

differential comparators built using a new Texas

Instruments developed low-voltage, high-speed bipolar process. These devices have been specifically developed for low-voltage, single-supply applications. Their enhanced performance makes them excellent replacements for the LM393 in today's improved 3-V and 5-V system designs.

The TLV1393, with its typical supply current of only 0.16 mA, is ideal for low-power systems. Response time has also been improved to 0.7 µs. For higher-speed applications, the TLV2393 features excellent ac performance with a response time of just 0.45 µs, three times that of the LM393.

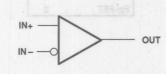
Package availability for these devices includes the TSSOP (thin-shrink small-outline package). With a maximum thickness of 1.1 mm and a package area that is 25% smaller than the standard surface-mount package, the TSSOP is ideal for high-density circuits, particularly in hand-held and portable equipment.

AVAILABLE OPTIONS

		PACKAGED D	EVICES			
TA	SUPPLY CURRENT (TYP)	RESPONSE TIME (TYP)	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
1000 1 10500	0.16 mA	0.7 μs	TLV1393ID	TLV1393IP	TL1393IPWLE	TLV1393Y
-40°C to 105°C	1.1 mA	0.45 μs	TLV2393ID	TLV2393IP	TLV2393IPWLE	TLV2393Y

PW packages are only available left-ended taped and reeled, (e.g., TLV1393IPWLE).

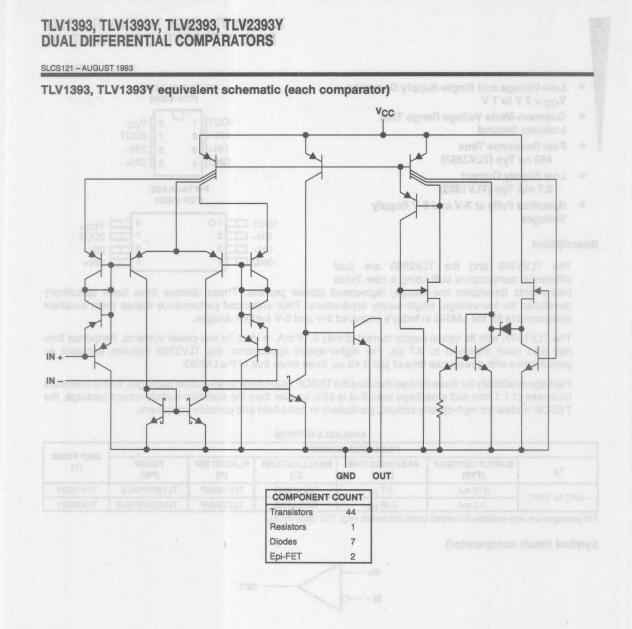
symbol (each comparator)



PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

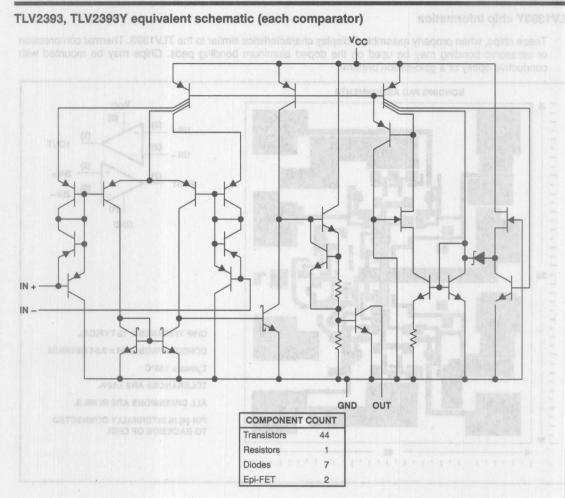


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TLV1393Y chip information

BONDING PAD ASSIGNMENTS Vcc -(8) literation of the lateration o (3) 1IN+ (6) (1) 10UT (2) 1IN-(5) 2IN+ 20UT (7) (6) 2IN-(4) GND (5) 11 - 38 Ti CHIP THICKNESS: 13 TYPICAL (4) BONDING PADS: 3.54 × 3.54 MINIMUM TJmax = 150°C 1.1.1.1.1 TOLERANCES ARE ±10%. ALL DIMENSIONS ARE IN MILS. **PIN (4) IS INTERNALLY CONNECTED** TO BACKSIDE OF CHIP. -32

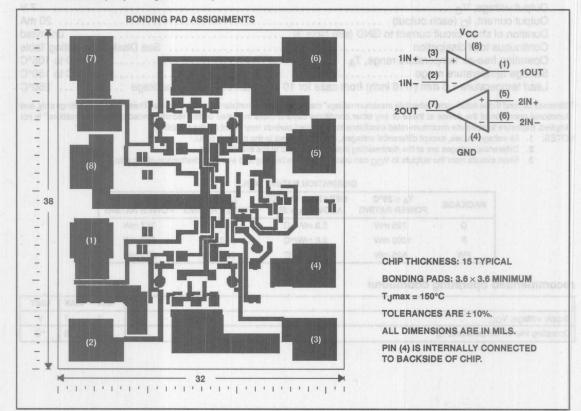
These chips, when properly assembled, display characteristics similar to the TLV1393. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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TYLV2393Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2393. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)
Differential input voltage, VID (see Note 2) 7 V
Input voltage, VI (any input)
Output voltage, V _O
Output current, I _O (each output)
Duration of short-circuit current to GND (see Note 3) unlimited
Continuous total dissipation
Operating free-air temperature range, T _A 40°C to 105°C
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network GND.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - 3. Short circuits from the outputs to V_{CC} can cause excessive heating and eventual destruction of the chip.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

recommended operating conditions

	MIN M.	AX UNIT
Supply voltage, V _{CC}	2	7 V
Operating free-air temperature, TA	-40 1	05 °C
PN (4) IS INTERNALLY CONNECTED		

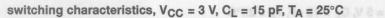


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	PARAMETER	TEST CONDITIONS					
			TA†	MIN.	TYP	MAX	UNIT
Vie	Input offset voltage		25°C		1.5	5	
VIO		$V_{O} = 1.4 V$, $V_{IC} = V_{ICR}min$	Full range		120	9	mV
Vion	Common mode input voltage range	25*0	25°C	0 to V _{CC} - 1.5	0 to V _{CC} -1.2		V
VICR	Common-mode input voltage range	Full range	Full range	0 to V _{CC} -2	er hogen skoten		V
VOL	Low-level output voltage	V _{ID} = -1 V, I _{OL} = 500 μA	Full range	6	120	300	mV
IIO	Input offset current	V _O = 1.4 V	25°C		5	50	- 0
			Full range		Mild and A	150	nA
	Innish bing assumed	25°C	25°C		-40	-250	- 4
IB	Input bias current	V _O = 1.4 V	Full range		DISTED	-400	nA
1	Liberts Incode an addition of a summark	V _{ID} = 1 V, V _{OH} = 3 V	25°C		0.1		- 0
IOH	High-level output current	V _{ID} = 1 V, V _{OH} = 5 V	Full range		uter tool inordetho.	100	nA
IOL	low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	500	cutput outrain	level-wo	μA
	internet internet internet internet	N. N.	25°C		160	250	
ICCH	High-level supply current	VO = VOH	Full range		IBURG Vicialities	300	1 HC
24	Low lovel events evenent	No. No.	25°C		160	250	μA
ICCL	Low-level supply current	VO = VOL	Full range		contra fuertas	300	

[†] Full range is -40°C to 105°C.

12 con manuel confiction



PARAMETER	TEST CONDITIONS		TLV1393			
PARAMETER			TYP	MAX	UNIT	
Response time	100-mV input step with 5-mV overdrive, RL connected to 5 V through 5.1 k Ω	ani Vini-0	0.7		μs	



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electrical characteristics, V_{CC} = 5 V (unless otherwise noted)

-	DADAMETED	TEST CONDITIONS	TA		10	UNIT	
	PARAMETER	TEST CONDITIONS	TAT	MIN	TYP	MAX	UNIT
	Input offect voltage		25°C		1.5	5	mV
VIO	Input offset voltage	$V_0 = 1.4 V$, $V_{IC} = V_{ICR}min$	Full range		Constant of the second	9	mv
Vien	Common-mode input voltage range	Orës	25°C	0 to V _{CC} – 1.5	0 to V _{CC} -1.2	Chime	V
VICR	Common-mode input voltage range	Poli range	Full range	0 to V _{CC} -2			V
VOL	Low-level output voltage	V _{ID} = -1 V, I _{OL} = 500 μA	Full range	ep:	120	300	mV
IIO	Input offset current	V _O = 1.4 V	25°C		5	50	-
			Full range		ningen verkellen eren	150	nA
lun An	Input bias current	V _O = 1.4 V	25°C		-40	-250	nA
IIB			Full range			-400	n/A
lau	High lovel output ourrent	V _{ID} = 1 V, V _{OH} = 3 V	25°C		0.1	interpretation	nA
ЮН	High-level output current	V _{ID} = 1 V, V _{OH} = 5 V	Full range			100	ΠA
IOL	Low-level output current	$V_{ID} = -1 V$, $V_{OL} = 1.5 V$	25°C	600	mus tucitos la	NUI-WOT	μA
laou	High-level supply current	No. No.	25°C	Inte	200	300	HØ
ICCH	High-level supply current	VO = VOH	Full range			350	
	Low-level supply current	Vo - Vo	25°C	E.S.S.	200	300	μA
ICCL	Low-level supply current	VO = VOL	Full range			350	

[†] Full range is -40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		Т	110.07		
	TESTCO	CONDITIONS		TYP	MAX	UNIT
Response time	100-mV input step with 5-mV overdrive,	R _L connected to 5 V through 5.1 k Ω	a Vm-00	0.65	8 million	nencque
	TTL-level input step,	R_L connected to 5 V through 5.1 k Ω	-	0.18		μs



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	PARAMETER		TEST CONDITIONS		TLV1393Y			
	PARAMETER				MIN	TYP	MAX	UNIT
VIO	Input offset voltage	25%	V _O = 1.4 V,	VIC = VICRmin		1.5	5	mV
VICR	Common-mode input voltage range	Full range	- (16) - (5)		0 to V _{CC} - 1.5	0 to V _{CC} -1.2		V
10	Input offset current		V _O = 1.4 V		-	5	50	nA
IIB	Input bias current	Prist month	V _O = 1.4 V			-40	-250	nA
ЮН	High-level output current	in the second	V _{ID} = 1 V,	VOH = 3 V		0.1		nA
IOL	low-level output current	0.02	$V_{ID} = -1 V$,	V _{OL} = 1.5 V	500	outout voltage	avel-wa	μΑ
ICCH	High-level supply current	aduation 1	VO = VOH	N 14 H GIN		160	250	
ICCL	Low-level supply current	0.05	Vo = Vol	Vatany		160	250	μA

switching characteristics, $V_{CC} = 3 V$, $C_L = 15 pF$, $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS		TLV1393Y		
PARAMETER			TYP	MAX	UNIT
Response time	100-mV input step with 5-mV overdrive, RL connected to 5 V through 5.1 k Ω	a ta	0.7	loval m	μs

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

Am	PARAMETER	TENT COMPLETIONS	1			
		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	$V_O = 1.4 V$, $V_{IC} = V_{ICR}min$		1.5	5	mV
VICR	Common-mode input voltage range	a 3 V, OL = 15 pF. TA = 15°C	0 to V _{CC} - 1.5	0 to V _{CC} -1.2	ng ch	V
10	Input offset current	V _O = 1.4 V		5	50	nA
IIB	Input bias current	V _O = 1.4 V		-40	-250	nA
ЮН	High-level output current	V _{ID} = 1 V, V _{OH} = 3 V	w moto towici l	0.1	consist of	nA
IOL	Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	600			μA
ІССН	High-level supply current	Vo = VoH		200	300	
ICCL	Low-level supply current	V _O = V _{OL}		200	300	μA

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV1393Y			
FARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
Response time	100-mV input step with 5-mV overdrive,	R _L connected to 5 V through 5.1 k Ω		0.65			
	TTL-level input step,	R_L connected to 5 V through 5.1 $k\Omega$		0.18		μs	



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electrical characteristics, V_{CC} = 3 V (unless otherwise noted)

	YERCEVUY	TEAT				TLV2393		UNIT
	PARAMETER	TEST CONDITIONS		TAT	MIN	ТҮР	MAX	UNIT
, Vim	1 3 A	0.001.00	Mar Marania	25°C		1.5	5	mV
VIO	Input offset voltage	$V_{O} = 1.4 V,$	VIC = VICRmin	Full range	adverse assured	Arrent choices	9	mv
An	08 8 9		VALEOV	25°C	0 to V _{CC} - 1.5	0 to V _{CC} -1.2	ello luci	V
VICR Common-mode input voltage range		Version	VA.F=OV	Full range	0 to V _{CC} -2	ไทร์ทมอ เมษายน เมษายน	Edd rog	V
1	Low lovel extent veltage	$V_{ID} = -1 V$,	I _{OL} = 1 mA	25°C		80	300	mV
VOL Low-level output voltage		$V_{ID} = -1 V$,	I _{OL} = 4 mA	Full range	100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100	250	700	IIIV
Law data the standard	V _O = 1.4 V	Jov vol	25°C		5	50	nA	
IIO Input offset current		$v_0 = 1.4 v$		Full range		and the second second second	150	1.114
	Input bies surrent	Va 14V	- T IN AL-	25°C	in V and	-100	-250	nA
IB	Input bias current	V _O = 1.4 V		Full range	and the second sec		-400	ΠA
TINU	High level output ourrent	V _{ID} = 1 V,	V _{OH} = 3 V	25°C		0.1	สราวณ	nA
OH	High-level output current	V _{ID} = 1 V,	V _{OH} = 5 V	Full range			100	ΠA
OL	low-level output current	$V_{ID} = -1 V$,	V _{OL} = 1.5 V	25°C	4	manut 1	100	mA
		No Nou		25°C		450	600	
CCH	High-level supply current	VO = VOH	: 25°C (unless	Full range	70		700	μA
	Low-level supply current	Vo = Vol	TRAT CON	25°C	and the second second	1.1	1.3	mA
CCL	Low-level supply current	VO = VOL	The second second	Full range			1.4	IIIA
Full rai	nge is -40°C to 105°C.	nimeouv - ouv	Wortz V			equility leaf	lo tuqni	

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

TEST CON	DITIONS	Т	LV2393	5 midate-	UNIT
TESTCON	DITIONS	MIN	TYP	MAX	UNIT
100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 $k\Omega$	NE CURI 91	0.45	1	μs
000 V C F H 10V		10010010	dino su	Locie	N.
		TEST CONDITIONS 100-mV input step with 5-mV overdrive, $\$ RL connected to 5 V through 5.1 k Ω	TEST CONDITIONS MIN	TEST CONDITIONS MIN TYP	MIN TYP MAX

witching characteristics, $V_{CC} = 5 V$, $C_L = 15 pF$, $T_A = 23^{\circ}C$



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TINU	DADAMETER	TEAT CONDITIONS		TLV2393			UNIT
	PARAMETER	TEST CONDITIONS	TAT	MIN	TYP	MAX	UNIT
Vin	Incuit offect voltage	Vo 14V Via Viarmin	25°C		1.5	5	mV
/IO Input offset voltage		$V_0 = 1.4 V$, $V_{IC} = V_{ICR}min$	Full range	in the second		9	mv
Vien	Common-mode input voltage range	Amit = jot . V f-= diV	25°C	0 to V _{CC} – 1.5	0 to V _{CC} -1.2	lievel-wc	V
VICR	Common-mode input voltage range	VAL-DV	Full range	0 to V _{CC} –2	t current	sello iog	V
10.00	Low-level output voltage	$V_{ID} = -1 V$, $I_{OL} = 1 mA$	25°C		70	300 mV	
VOL	Low-level output voltage	$V_{ID} = -1 V$, $I_{OL} = 4 mA$	Full range		200	700	mv
in Au	Input offset current	V _O = 1.4 V	25°C		5	50	nA
10	input onset current	VO = 1.4 V	Full range			150	IIA
	Input bias current	V _O = 1.4 V	25°C		-100	-250	nA
IB	input bias current	VO = 1.4 V	Full range	in se an	Contractor to a	-400	IIA
	High-level output current	V _{ID} = 1 V, V _{OH} = 3 V	25°C		0.1		nA
ЮН	High-level output current	V _{ID} = 1 V, V _{OH} = 5 V	Full range			100	nA
OL	low-level output current	$V_{ID} = -1 V$, $V_{OL} = 1.5 V$	25°C	6	and the second second		mA
0.011	High-level supply current	No. Nou	25°C	w cinte undra /	550	700	
CCH	Figh-level supply current	VO = VOH	Full range			800	μА
001	Low-level supply current	Vo = Vol	25°C	a opvies	1.2	1.5	mA
ICCL	Low-level supply current	VO = VOL	Full range			1.6	MA

[†] Full range is -40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CO	NDITIONS	TLV2393	LINUT
PARAMETER	TEST CO	NDITIONS	MIN TYP MAX	UNIT
Act 08	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 k Ω	0.4 0.8	0
Response time	TTL-level input step,	R_L connected to 5 V through 5.1 $k\Omega$	0.15 0.3	μs
	10 VC+PCV	NI ~ div	themics fuctive level - of H	HC

performing characteristics, Vec. = 5 V. Ci = 15 pF. Ti = 25°C.

	TEST CONDITIONS	



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electrical characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

	ERESV.IT	TEST CONDITIONS		1	LV2393Y	12.	UNIT
	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	25°O	Vo = 1.4 V, VIC = VICRmin		1.5	5	mV
VICR	Common-mode input voltage range	Pull range	100 - 00 - 10 - 00	0 to V _{CC} - 1.5	0 to V _{CC} -1.2		V
VOL	Low-level output voltage	0.03	$V_{ID} = -1 V$, $I_{OL} = 1 mA$		80	300	mV
10	Input offset current	annin luit.	V _O = 1.4 V		5	50	nA
IIB	Input bias current		V _O = 1.4 V		-100	-250	nA
ЮН	High-level output current	2010	V _{ID} = 1 V, V _{OH} = 3 V	00	0.1	Low-les	nA
IOL	low-level output current	Egner aura	V _{ID} = -1 V, V _{OL} = 1.5 V	4			mA
ICCH	High-level supply current	0.63	Vo = VoH		450	600	μA
ICCL	Low-level supply current	n Kunsa un a	V _O = V _{OL}		1.1	1.3	mA

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	na suo TI	LV23931	el-digit-la	UNIT
PARAMETER	TEST CONDITIONS		TYP	MAX	UNIT
Response time	100-mV input step with 5-mV overdrive, $\ \mbox{R}_L$ connected to 5 V through 5.1 k Ω		0.45	1	μs

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

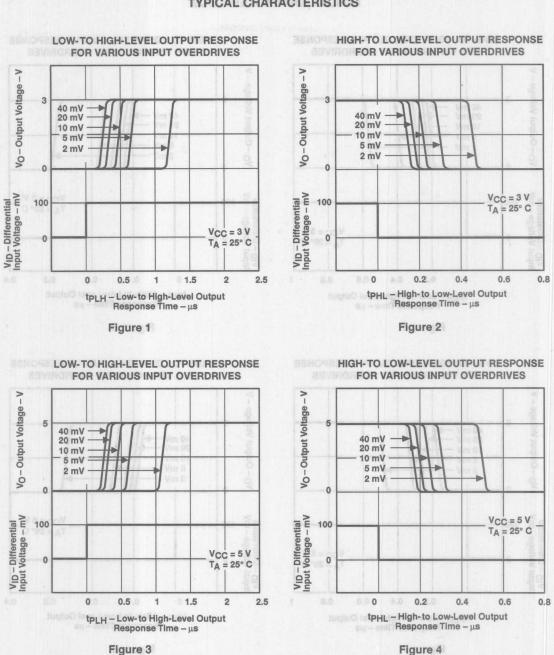
	BADAMETER	TEST CONDITIONS	1	LV2393Y		LINUT
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	$V_O = 1.4 V$, $V_{IC} = V_{ICR}min$		1.5	5	mV
VICR	Common-mode input voltage range	er = Vi Aif ei = Te Vi ei	0 to V _{CC} – 1.5	0 to V _{CC} -1.2	and fill	V
VOL	Low-level output voltage	$V_{ID} = -1 V$, $I_{OL} = 1 mA$		70	300	mV
10	Input offset current	V _O = 1.4 V	INV ORTA THERE	5	50	nA
IB	Input bias current	V _O = 1.4 V	asin tuoni k	-100	-250	nA
ЮН	High-level output current	V _{ID} = 1 V, V _{OH} = 3 V		0.1		nA
IOL	low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	6			mA
ССН	High-level supply current	Vo = VoH		550	700	μA
ICCL	Low-level supply current	V _O = V _{OL}		1.2	1.5	mA

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CON	IDITIONS	Т	LV23931	1	UNIT
PANAMETER	TESTCO	TEST CONDITIONS		TYP	MAX	UNIT
Dente	100-mV input step with 5-mV overdrive,	RL connected to 5 V through 5.1 k Ω		0.4	0.8	
Response time	TTL-level input step,	R_L connected to 5 V through 5.1 $k\Omega$		0.15	0.3	μs



SLCS121 - AUGUST 1993



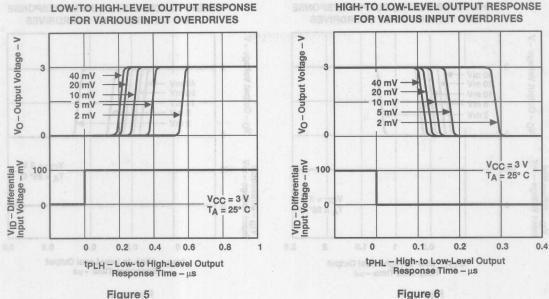
TYPICAL CHARACTERISTICS



3-15

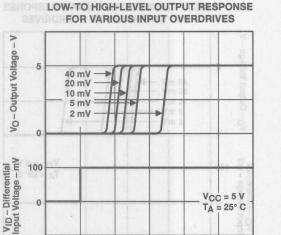
SLCS121 - AUGUST 1993

TYPICAL CHARACTERISTICS

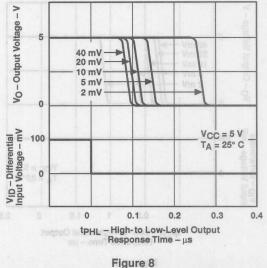














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VCC = 5 V

TA = 25° C

0.8



0

0

0.2

Figure 7

0.4

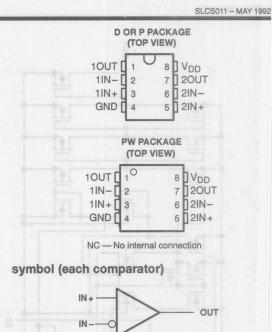
tpLH – Low- to High-Level Output Response Time – μs

0.6

- Wide Range of Supply Voltages 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Very-Low Supply-Current Drain 120 μA Typ at 3 V
- Output Compatible With TTL, MOS, and CMOS
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- High Input Impedance . . . 10¹² Ω Typ
- Extremely Low Input Bias Current 5 pA Typ
- Common-Mode Input Voltage Range Includes Ground
- Built-In ESD Protection

description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μ A.



The TLV2352 is designed using the Texas Instruments LinCMOSTM technology and therefore features an extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352 is fully characterized at 3 V and 5 V for operation from – 40°C to 85°C.

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

	N	PA	CKAGED DEVICE	S	CHIP
TA	VIOmax at 25°C	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	FORM (Y)
-40°C to 85°C	5 mV	TLV2352ID	TLV2352IP	TLV2352IPWLE	TLV2352Y

.....

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR) PW packages are only available left-ended taped and reeled, (e.g., TLV2352IPWLE)



Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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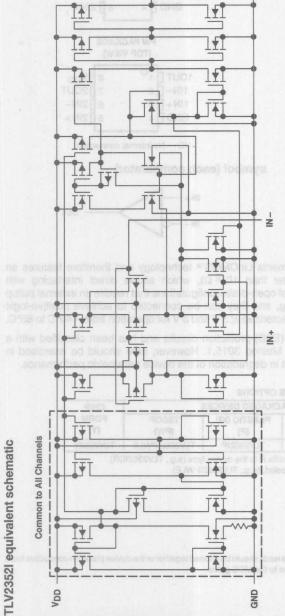
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SLCS011 - MAY 1992

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The TLV2352 has internal electrostatio-discharge (Es 2000-V ESD rating tested under MiL-STD-8830, Mar



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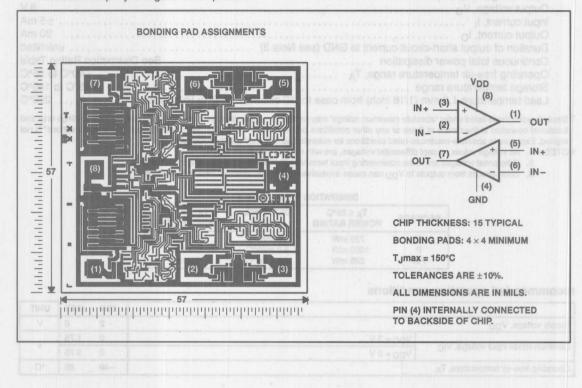
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TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VDD (see Note 1)	
Differential input voltage, VID (see Note 2)	
Input voltage range, V ₁	
Output voltage, Vo	8 V
Input current, I	±5 mA
Output current, Io	
Duration of output short-circuit current to GND (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, TA	40°C to 85°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or F	PW package 260°C

[†] Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

- 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
- 3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

	DISSIPATION	RATING TABLE	
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

NTERMALLY CONNECTED	(a) MP	fillen stelen	MIN	MAX	UNIT
Supply voltage, VDD	DAS OT		2	8	V
Common-mode input voltage, VIC	V _{DD} = 3 V	and the present of the state of	0	1.75	V
	V _{DD} = 5 V		0	3.75	V
Operating free-air temperature, TA				. 85	°C



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		BOSILEY					TLV2	3521		R. Harris		
	PARAMETER	TEST CO	ONDITIONS	T _A ‡	V	DD = 3 \	1	V _{DD} = 5 V			UNIT	
		N KASE OY			MIN	TYP	MAX	MIN	TYP	MAX		
	Innut offerst veltage	out offset voltage VIC = VICBmin, See Note 4		25°C	Victoria	-01/1	5		1	5	mV	
VIO	Input offset voltage	AIC = AICBuilt	I, See Note 4	Full range			7		nemus la	7	mv	
IO Input offset current	5		25°C		1			1	asid tug	pА		
10	Input onset current	0		85°C			1	dellow fue	ni oban	1	nA	
An		1,0		25°C	' Vr	5	1.00	Ineral	5	svel-rip	pА	
IB	Input bias current	A		85°C	Vi-	- ny T	2	otacia	v fuetuci	2	nA	
Arte 81.	8 8 8 8 8 8 V		25°C	0 to 2	-mv1		0 to 4	o tuatoo	lavel-wit			
VICR	Common-mode input voltage range	120 250		Full range	0 to 1.75	= avi		0 to 3.75	hen	uo yigqi	V	
NE	High-level output	N. AN	NOTING THE OLIDARY	25°C	av muni	0.1	Ven are	a limita o	0.1	he offer	nA	
ОН	current	V _{ID} = 1 V		Full range	eril beev	what note	ine Of	of a clinw	Vm:00+	wolectra	μA	
	Low-level output	No. 4 M	1 00	25°C		115	300	ander intels	150	400		
VOL	voltage	$V_{ID} = -1 V,$	$I_{OL} = 2 \text{ mA}$	Full range			600			700	mV	
OL	Low-level output current	V _{ID} = -1 V,	V _{OL} = 1.5 V	25°C	6	16		6	16		mA	
	Cumply summert	N= 11	No lood	25°C		120	250		140	300		
DD	Supply current	V _{ID} = 1 V, No load		Full range			350			400	- μΑ	

[†] All characteristics are measured with zero common-mode input voltages unless otherwise noted.

[‡] Full range is -40°C to 85°C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with VDD = 5 V, 2 V with VDD = 3 V, or below 400 mV with a 10-kΩ resistor between the output and VDD. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS						UNIŢ
Response time	R _L = 5.1 kΩ,	CL = 15 pF§,	See Note 5	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		Т	UNIT					
PARAMETER			TEST CONE	DITIONS	MIN	TYP	MAX	UNIT
Response time	PL 51KO	0. 15 - 58	0	100-mV input step with 5-mV overdrive	650		ns	
	$R_{L} = 5.1 \text{ k}\Omega, C_{L} = 15 \text{ pF}\$,$	See Note 5	TTL-level input step		200			

§ CL includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses Vo = 1 V with $V_{DD} = 3 V \text{ or } V_O = 1.4 V \text{ with } V_{DD} = 5 V.$



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electrical characteristics at specified free-air temperature, T_A = 25°C[†]

	NLV2362I				4	TLV2	352Y			
	PARAMETER	TEST CON	V	DD = 3 \	1	V _{DD} = 5 V			UNIT	
		177 HBM		MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	VIC = VICRmin,	See Note 4	Can Alexan	1	5		1	5	mV
10	Input offset current		gran lluri		1			1		pА
IIB	Input bias current		1 25.0		5		1.1	5	Law and	pА
VICR	Common-mode input voltage range		0.40	0 to 2			0 to 4			V
ЮН	High-level output current	V _{ID} = 1 V	1 2610		0.1			0.1	anist has	nA
VOL	Low-level output voltage	$V_{ID} = -1 V$	$I_{OL} = 2 \text{ mA}$		115	300		150	400	mV
IOL	Low-level output current	$V_{ D} = -1 V$,	V _{OL} = 1.5 V	6	16	1.11	6	16		mA
IDD	Supply current	V _{ID} = 1 V	No load		120	250		140	300	μА

[†] All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with $V_{DD} = 5 V$, 2 V with $V_{DD} = 3 V$, or below 400 mV with a 10-k Ω resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

	- 001	 000			,V 1 - = 01V	

All characteristics are mediculed with zero common mode input volgiges unless clinerwise nore

a construction in automore and an entropy and a set a real transitional "Ouce of Ouce- at 60 to 10-14

OTE at: The other voltage innuin given and the monthium version requests to drive the output exclose 4.9 with VDD = 3.9, 2.9 with VDD = 3.9, 2.9 with 400 mV with a 10-600 resister between the output and VDD. They as a be writted by applying the link value to the input and ender the version of the link track.

withhin abaratations Vene 3 V.T. - 25

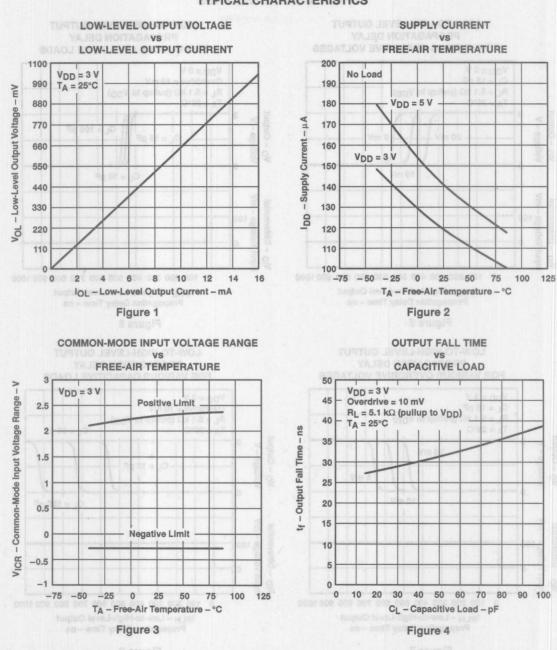
initiohing characteristics, $V_{DD} = 5 V$, $T_{A} = 25^{\circ}C$

Or Includes probe and its capacitarica.

NOTE 5: The response time specified is the interval between the input stop function and the instant when the output crosses Vo = 1.V with Vop = 8.V or Vo = 1.4.V with Vop = 6.V.



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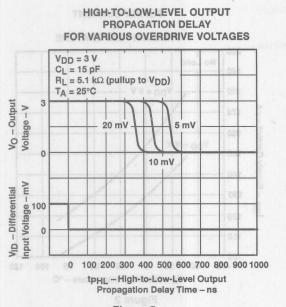
TYPICAL CHARACTERISTICS



3-23

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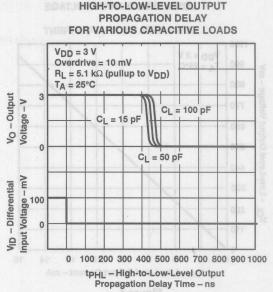


Figure 5



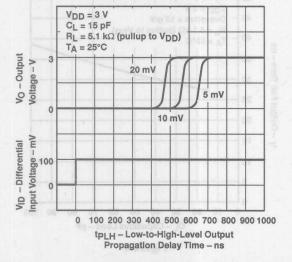


Figure 7

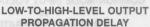
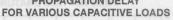


Figure 6



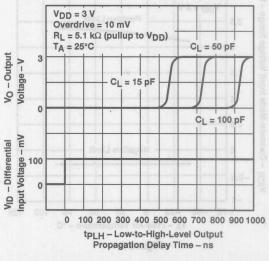


Figure 8



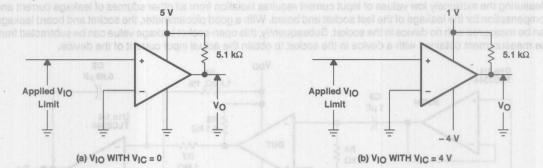
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PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.





A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.



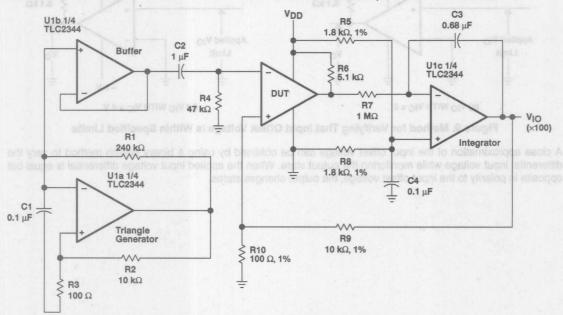
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PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.





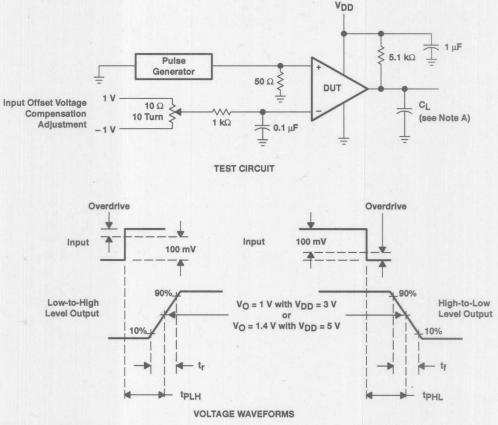


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PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses $V_0 = 1 V$ with $V_{DD} = 3 V$ or when the output crosses $V_0 = 1.4 V$ with $V_{DD} = 5 V$. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



NOTE A: CL includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

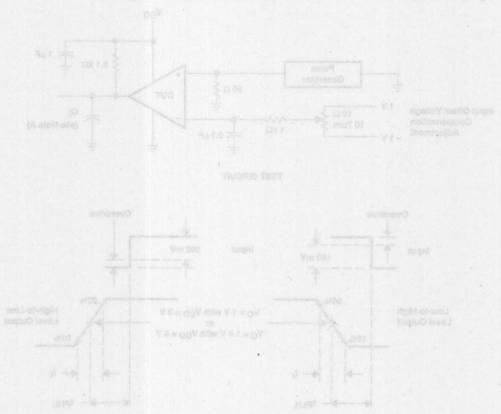


TLV23521, TLV2352Y LINCMOSTH DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

BLCSOTT - MAY 198

PARAMETER MEASUREMENT WEORMATION

Propagation delay time is defined as the fatiantal between the application of an input step function and the instant when the output arceses $V_D = 1.7 \text{ with } V_{DD} = 2.7 \text{ or when the output crosses } V_D = 1.4 V with <math>V_{DD} = 5.7$. Propagation delay time, low-to-high-level output, is measured from the leading adge of the input pulse while propagation delay time high-to-iow-level output, is measured from the trailing adge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low stonal, for example 105-fity or 5-mV overderve, causes the output to drame states.



PREPARE VENUERORIES

NOTE A: Or includes probe and jip department.

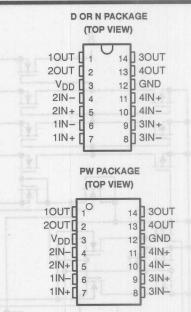
Figure 11, Propagation Delay, Rise, and Fail Timos Test Climpit and Voltage Waveforms

- Wide Range of Supply Voltages
 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Very-Low Supply-Current Drain 240 μA Typ at 3 V
- Common-Mode Input Voltage Range
 Includes Ground
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- High Input Impedance ... 10¹² Ω Typ
- Extremely Low Input Bias Current 5 pA Typ
- Output Compatible With TTL, MOS, and CMOS
- Built-In ESD Protection

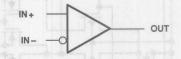
description

The TLV2354 consists of four independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 240 μ A.

The TLV2354 is designed using the Texas Instruments LinCMOSTM technology and therefore features an extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interfacing with high-impedance sources. The



symbol (each comparator)



outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2354 is fully characterized for operation from – 40°C to 85°C.

The TLV2354 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

	Manager	PA	CHIP		
TA	VIOmax at 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	FORM (Y)
-40°C to 85°C	5 mV	TLV2354ID	TLV2354IN	TLV2354IPWLE	TLV2354Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR). PW packages are only available left-ended taped and reeled, (e.g., TLV2354IPWLE)



Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Wide Range of Supply Voltages
 2 V to 8 V

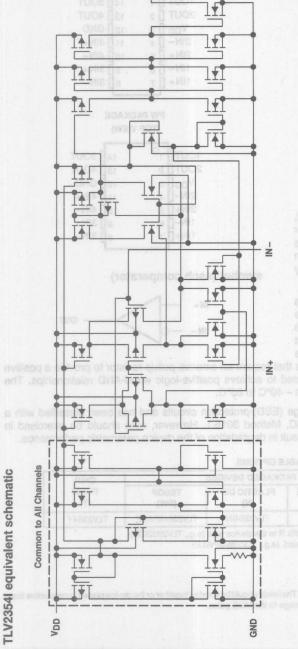
- Fully Characterized at 3 V and 5 V
- Very-Low Supply-Current Drain
 240 pA Typ at 3 V
- Common-Mode Input Voltage Pang-Includes Ground
- Fast Response Time . . . 200 na Typ for TTL-Level Input Step
 - (F O 2101 eonebegmi tugni dgiH *
 - Extremely Low Input Blas Current
 5 pA Typ
- Output Compatible With TTL, MOS, and CMOS
 - Built-in ESD Protection

description-

The TLV2364 constats of four tadependent, low-power comparators spacifically designed for single power-supply applications and to operate with power-supply raits as low as 2 V. When powered from a 3-V supply, the typical supply current is only 240 µA.

The TUV2354 is designed using the Texas instruments LinDMOST* technology and therefore features an extremely high input importance. (typically greater than 10¹² Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations to output voltage swing, and they can be connecte TI.V2354 is fully characterized for operation from -

The TLV2354 has internal electrostatio-discharge (ESI 2000-V ESD rating tasted under MiL-STD-883C. Meth handling this device as excessive to ESD may result in d



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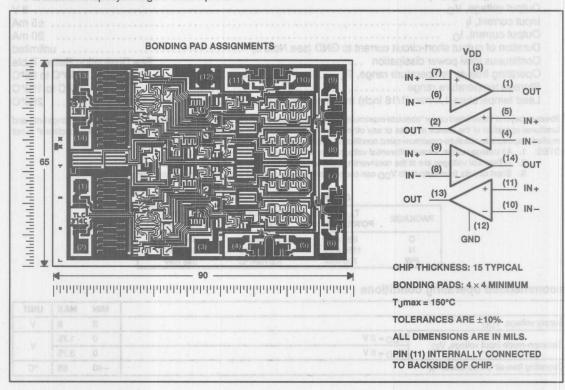
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TLV2354Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2354. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, VDD (see Note 1)
Differential input voltage, VID (see Note 2)
Input voltage range, V ₁ –0.3 to 8 V
Output voltage, V _O
Input current, I ₁
Output current, I _O
Duration of output short-circuit current to GND (see Note 3)
Continuous total power dissipation
Operating free-air temperature range, T _A
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package 260°C

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

	DISSIPATION	RATING TABLE	
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	T _A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	346 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, VDD	2	8	V	
Common-mode input voltage, VIC	V _{DD} = 3 V	0	1.75	V
	V _{DD} = 5 V	0	3.75	V
Operating free-air temperature, TA	-40	85	°C	



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		TEST CONDITIONS			TLV2354I						
	PARAMETER			TA‡	VESTO	DD = 3 \	1	V	DD = 5 V	(d)	UNIT
		TVP MAL			MIN	TYP	MAX	MIN	TYP	MAX	
Vm	langest offerst voltages	fset voltage V _{IC} = V _{ICR} min, See Note 4		25°C	MADIY	- OV1	5	1	gallo 18	5	
VIO	input onset voitage			Full range			7	1.1	nemus, In	7	mV
Ac	Input offset current	5		25°C		1			lasm1.	sid hay	pA
10	IO input onset current	0		85°C			igran 1g	ation luc	ni sibom-	eemin 1 0	nA
An	In the line of the set	0.1		25°C	V F.	5		merna	5	svel-ng/	pA
IB	IB Input bias current	115 '300		85°C	VIA	- avl	2	oltaga	v suglad i	2	nA
VICR voltage range	V 6 16		25°C	0 to 2	- divi		0 to 4	o tughia i	evol-wa	1	
	240 800		Full range	0 to 1.75	- diV	rear di	0 to 3.75	interni anter entre		V	
190 V 8	High-level output	igh-level output urrent VID = 1 V		25°C	less resurts	0.1	ens nev	g atiriti c	0.1	Fha offa	nA
ЮН	current	$ \Lambda D = 1 \Lambda$		Full range	0 em 18	ewise to	1	-01 8 10	W.Vm Co	1	μA
Val	Low-level output			25°C		115	300		150	400	
VOL	voltage	$V_{ID} = -1 V$,	$I_{OL} = 2 \text{ mA}$	Full range			600	1.5-1.47.5		700	mA
IOL	Low-level output current	V _{ID} = -1 V,	V _{OL} = 1.5 V	25°C	6	16		6	16		mA
	Sumply summent	N= 11	Neleed	25°C		240	500		290	600	
DD	DD Supply current	$V_{1D} = 1 V,$	No load	Full range			700			800	μA

[†] All characteristics are measured with zero common-mode input voltage unless otherwisé noted.

[‡] Full range is -40°C to 85°C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER		Т					
PARAMETER				MIN	TYP	MAX	UNIT
Response time	R _L = 5.1 kΩ, See Note 5	C _L = 15 pF§,	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		Т	110117				
PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
Response time	$ \begin{array}{ll} R_{L} = 5.1 \; k\Omega, & C_{L} = 15 \; pF\$, \\ \text{See Note 5} \end{array} $		100-mV input step with 5-mV overdrive	ve 650 200			
			TTL-level input step				ns

§ C1 includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.



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	TLV23841			TLV2354Y						
	PARAMETER	TEST CONDITIONS		V _{DD} = 3 V			V _{DD} = 5 V			UNIT
		VT BIN		MIN	TYP	MAX	MIN	TYP	MAX	
VIO	Input offset voltage	VIC = VICRmin,	See Note 4		1	5		1	5	mV
IIO	Input offset current	6	price Built		1	cox Ca		1		pА
IIB	Input bias current		25°C		5			5	Sec. Sec.	pА
VICR	Common-mode input voltage range		0*88	0 to 2			0 to 4			V
ЮН	High-level output current	V _{ID} = 1 V	0*85		0.1			0.1	and have	nA
VOL	Low-level output voltage	$V_{ID} = -1 V$	IOL = 2 mA		115	300		150	400	mV
IOL	Low-level output current	$V_{ID} = -1 V$,	VOL = 1.5 V	6	16		6	16	- non ma	mA
IDD .	Supply current	VID = 1 V	No load		240	500	1	290	600	μА

electrical characteristics at specified free-air temperature, T_A = 25°C[†]

[†] All characteristics are measured with zero common-mode input voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

	150	 300				

As presedurinance are measured with zero common-modul input variage unless conervise in

+ Pull range is - 40°C to 85°C. NePOHTANT: See Parameter Messurement Information.

VE 4: The other voltage limits given are the maximum values required to over the output above 4.9 with VDD = 5.4, 2.9 with VDD = 3.9, or bolow 400 mV with a 10-400 restator between the output and VDD. They can be verified by applying the limit value to the input and other details accomputed where

switching characteristics, Vop = 3 V, TA = 25°C

TLV23540 NBN TYP MAX	

switching characteristics, Vnn = 5 V. Ta = 25°C

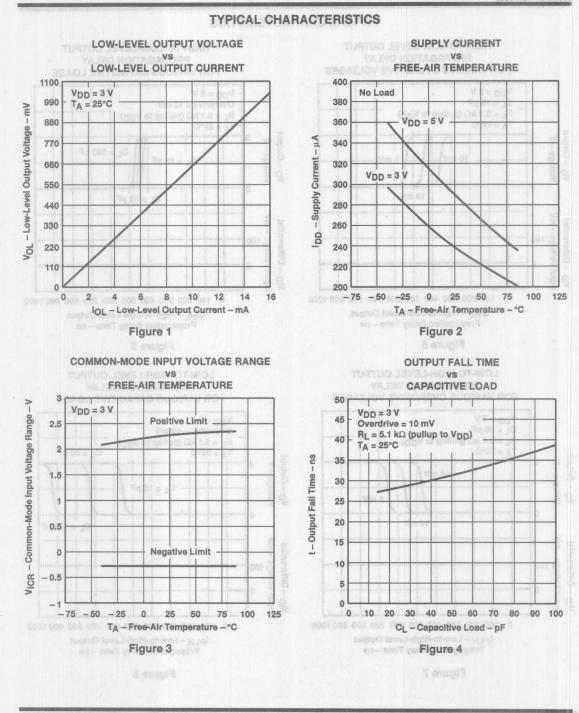
	080 005	grinderte titrertern spile i		

\$ C) Includes probe and lig capacitupos.

DTE Sr. The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{OD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.



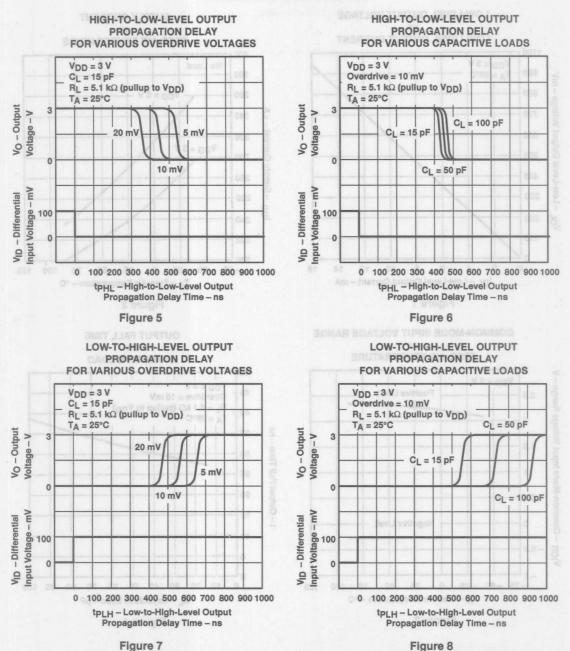
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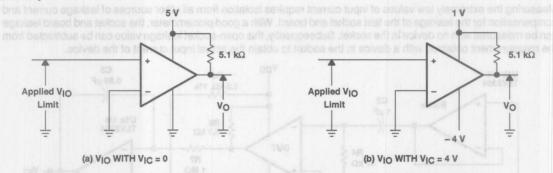
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PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test rather than changing the input voltages to provide greater accuracy.





A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.



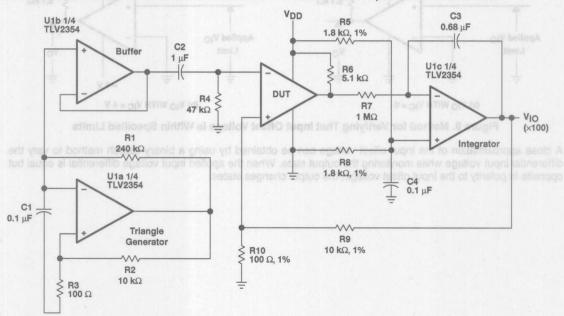
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PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.



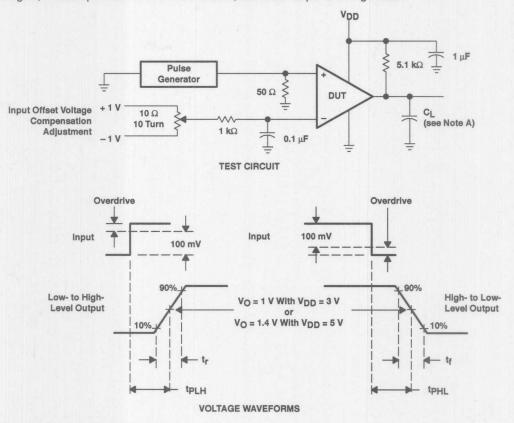


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PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses $V_0 = 1 V$ with $V_{DD} = 3 V$ or when the output crosses $V_0 = 1.4 V$ with $V_{DD} = 5 V$. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, cause the output to change state.



NOTE A: CL includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

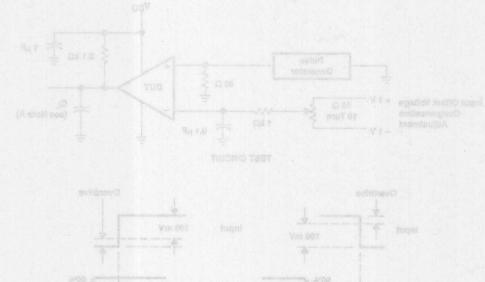


TLV2354, TLV2354Y LincMOS^{T*} QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval fatiwaen the application of an input step function and the instant when the output crosses $V_{\rm O} = 1 V$ with $V_{\rm OD} = 3 V$ or when the output crosses $V_{\rm O} = 1.4 V$ with $V_{\rm DD} = 5 V$. Propagation delay time, low-to-nigh-level output, is measured from the leading edge of the input putse, while propagation delay time high-to-low-level output, is measured from the trailing edge of the input putse, while propagation delay time as frow input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the oncut is just at the transition point. Ther a low signal, for example 105-mV or 5-mV overdrive, cause the opticul to drange state.





NOTE A: OL Indudes proba and its capacitance.

Figure 11, Propagation Datay, Fise, and Fall Timos Test Circuit and Voltage Waveforms



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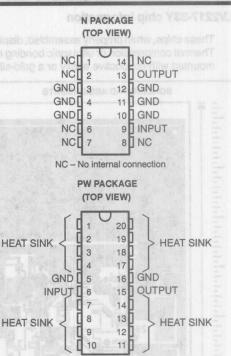
- Fixed 3.3-V Output
- ±1% Maximum Output Voltage Tolerance at T_J = 25°C
- 500-mV Maximum Dropout Voltage at 500 mA
- 500-mA Dropout Current
- ±2% Absolute Output Voltage Variation
- Internal Overcurrent Limiting
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

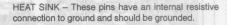
description

The TLV2217-33 is a low-dropout 3.3-V fixed voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V or less. The TLV2217-33 provides internal overcurrent limiting, thermal-overload protection, and overvoltage protection.

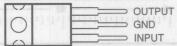
The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator may drop as low as 3.8 V, and the TLV2217-33 will continue to regulate the system. For higher voltage systems, the TLV2217-33 may be operated with a continuous input voltage of 12 V.

The TLV2217-33N and TLV2217-33KC cannot be harmed by temporary mirror-image insertion. This regulator is characterized for operation from 0°C to 125°C virtual junction temperature.

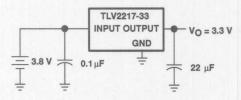








application schematic



AVAILABLE OPTIONS

	P	CHIP		
TJ	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)	FORM (Y)
0°C to 125°C	TLV2217-33KC	TLV2217-33N	TLV2217-33PWLE	TLV2217-33Y

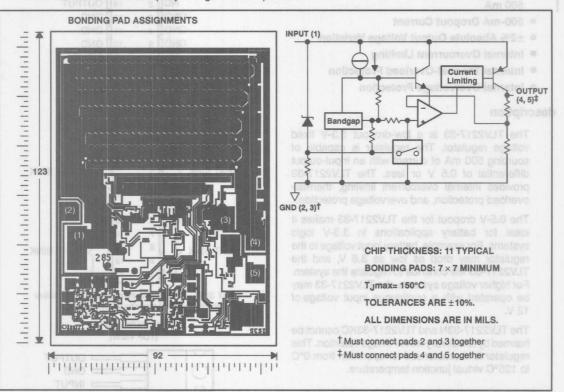
The PW package is only available left-end taped and reeled.

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TLV2217-33Y chip information



These chips, when properly assembled, display characteristics similar to the TLV2217-33 (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



IEXAS INSTRUMENTS

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absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

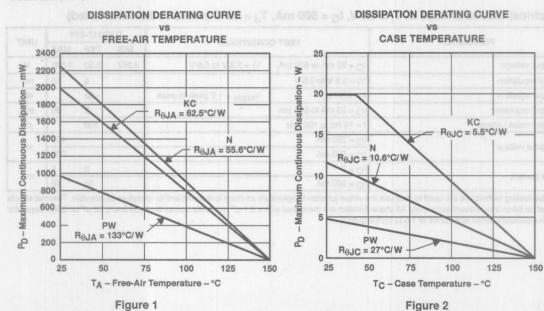
Continuous input voltage	16 V
Continuous total dissipation (see Note 1)	See Dissipation Rating Table
Operating virtual junction temperature range	
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	TA	2000 mW	16.0 mW/°C	1280 mW	1040 mW	400 mW
	TC [†]	20000 mW	182.0 mW/°C	14540 mW	11810 mW	4645 mW
N	TA	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	TC	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	TA	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	TC	4625 mW	37.0 mW/°C	2960 mW	2405 mW	925 mW

[†] Derate above 40°C





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recommended operating conditions	MIN	MAX	UNIT
Input voltage, VI egsilov	3.8	12	V
Output current, IO and and an	0	500	mA
Operating virtual junction temperature range, TJ			°C

electrical characteristics at VI = 4.5 V, IO = 500 mA, TJ = 25°C (unless otherwise noted)

DADAMETED	TEST CONDITIONST		TLV2217-			
PARAMETER			MIN TYP	MAX	UNIT	
Output vicitage	$I_{O} = 20 \text{ mA to } 500 \text{ mA},$ $V_{I} = 3.8 \text{ V to } 5.5 \text{ V}$	TJ = 25°C	3.267 3.30	3.333	V	
Output voltage		TJ = 0°C to 125°C	3.234	3.366		
Input regulation	V _I = 3.8 V to 5.5 V		5	15	mV	
Ripple rejection	f = 120 Hz,	Vripple = 1 V peak-to-peak	-62		dB	
Output regulation	I _O = 20 mA to 500 mA		5	30	mV	
Output noise voltage	f = 10 Hz to 100 kHz	0.01	500	territoria da constante	μV	
Dropout voltage	I _O = 250 mA			400	mV	
Dropout voltage	I _O = 500 mA	2.2. Islan 22.0		500	00	
Bias current	IO = 0		2	5	mA	
Dias current	I _O = 500 mA		19	49		

electrical characteristics at VI = 4.5 V, IO = 500 mA, TJ = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLV2217-33Y			
PARAMETER			MIN	TYP	MAX	UNIT
Output voltage	I _O = 20 mA to 500 mA,	VI = 3.8 V to 5.5 V	3.267 3.30	3.30	3.333	V
Input regulation	V _I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz,	Vripple = 1 V peak-to-peak		-62	1	dB
Output regulation	I _O = 20 mA to 500 mA	PLA = 02.5 C/W		5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz		25	500		μV
Dropout voltage	I _O = 250 mA	N. Antonio	fait	-	400	mV
Dropoul voltage	I _O = 500 mA	Monoral = West	have		500	mv
Bias current	IO = 0	and and the		2	5	
bias current	l _O = 500 mA			19	49	mA

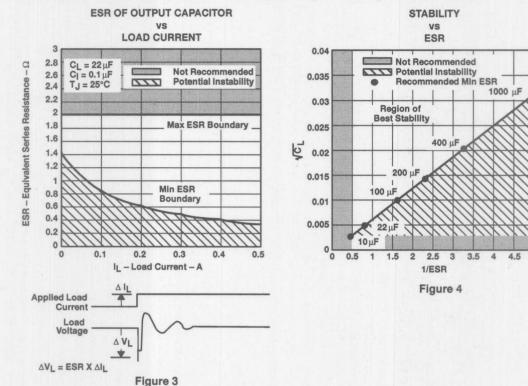
[†] Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.



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COMPENSATION-CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.





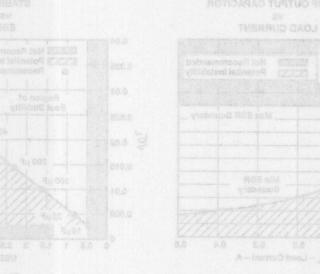
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TLV2217-33, TLV2217-33, TLV2217-33, TLV2217-33Y LOW-DROPOUT 3.3-V FIXED VOLTAGE REGULATORS

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COMPENSATION-CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor velue and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load runga and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.





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Comparators

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- Low r_{DS(on)} . . . 0.18 Ω Typ at V_{GS} = -10 V
- 3-V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- V_{GS(th)} = -1.5 V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protected

description

The TPS1100 is a single p-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOSTM process. With a maximum V_{GS}(th) of -1.5 V and an I_{DSS} of only 0.5 μ A, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low r_{DS}(on) and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin TSSOP (PW) version, with its smaller footprint and reduction in height, fits in places where other p-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for an SOIC package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

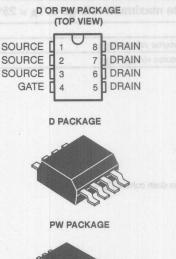
AVAILABLE OPTIONS

UA = 248°C/W	PACKAGED DEVICEST				
TJ	SMALL OUTLINE (D)	TSSOP (PW)			
-40°C to 150°C	TPS1100D	TPS1100PWLE			

[†] The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE).

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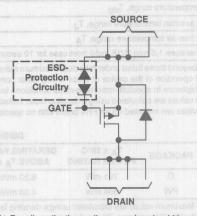
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schematic

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NOTE: For all applications, all source pins should be connected and all drain pins should be connected.



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gang comparing provide	States and the		old.	maqmod vi	UNIT
Drain-to-source voltage, VDS		50	External V	-15	V
Gate-to-source voltage, VGS		stugni eidi	08 Campal	2, -15	V
SOURCE [] 3 B [] DRAIN			T _A = 25°C	±0.41	1.0
	V _{GS} = -2.7 V	D package	T _A = 125°C	±0.28	
	V _{GS} = -2.7 V	DW/ package	T _A = 25°C	±0.4	
		PW package	T _A = 125°C	±0.23	
		Dinaskana	T _A = 25°C	±0.6	sorig
Continuous drain current (TJ = 150°C), ID [‡]		D package	T _A = 125°C	±0.33	
		PW package	$T_A = 25^{\circ}C$	±0.53	
			T _A = 125°C	±0.27	
	V _{GS} = -4.5 V	D package	T _A = 25°C	ewe±1,eet	sd A
			T _A = 125°C	±0.47	sent (sm 3.0
		PW package	T _A = 25°C	±0.81	
			T _A = 125°C	±0.37	
	menneger	D package	T _A = 25°C	±1.6	101
	$V_{GS} = -10 V$		T _A = 125°C	±0.72	200
	VGS = - 10 V	PW package	T _A = 25°C	±1.27	inn
and the second se	enetiment	F vv package	T _A = 125°C	±0.58	eT.
Pulsed drain current, IDM [‡]	Atohes for	ia tewoo an i	cations such	±7	A
Continuous source current (diode conduction), IS	oliers or sch	WND contr	odulated (m-rtibit/-sa	A
Storage temperature range, T _{Stg}			rivers.	-55 to 150	°C
Operating junction temperature range, TJ	ell ruhw	nolensy (W	TSSOP (P	-40 to 150	°C
Operating free-air temperature range, TA	ni titi in	ction in help	in and redu	-40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 second	ds donneo d	T3R2OM len	other p-chan	260	°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

* Maximum values are calculated using a derating factor based on R_{0JA} = 158°C/W for the D package and R_{0JA} = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR [‡] ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/°C	323 mW	262 mW	100 mW

[‡] Maximum values are calculated using a derating factor based on R_{θ JA} = 158°C/W for the D package and R_{θ JA} = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

-40°C to 160°C TP81100D TP81100PWLE The D package is invaliable (ap-ed and realed. Advi an R auth to device type (a.g., TPS11000F). The PW package is avritable only left-end taped and market (indicated by the LP suffix on the device type; e.g., TPS1100PWLE).

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5-4

SLVS078A - DECEMBER 1993 - REVISED FEBRUARY 1994

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			MIN TY	P MAX	UNIT			
VGS(th)	Gate-to-source threshold voltage	VDS = VGS,	I _D = -250 μA		-1 -1.2	25 -1.50	V			
VSD	Source-to-drain voltage (diode forward voltage) [†]	I _S = -1 A, V _{GS} = 0 V			.9	V				
IGSS	Reverse gate current, drain short circuited to source	V _{DS} = 0 V, V _{GS} = -12 V		Static dis	±100	nA				
	Zere entr voltage drain ovrant	V 10V	V 10.V	Vac 10V Va	Var 10V V	Ver OV	TJ = 25°C	Statio din	-0.5	
DSS	Zero-gate-voltage drain current	$v_{DS} = -12 v,$	$V_{DS} = -12 V$, $V_{GS} = 0 V$		Source-h	-10	μA			
	R apploy equilit	VGS = -10 V	$I_{D} = -1.5 A$	in-to-source on-si	no share 18	30				
	and the second s	VGS = -4.5 V	$I_{D} = -0.5 \text{ A}$		29	91 400				
rDS(on)	Static drain-to-source on-state resistance [†]	$V_{GS} = -3 V$	spaliny amu		s-of-ateo 4	76 700	mΩ			
		$V_{GS} = -3 V$ $V_{GS} = -2.7 V$	$I_{D} = -0.2 \text{ A}$. 60	06 850				
gfs	Forward transconductance [†]	$V_{DS} = -10 V_{,}$	$I_D = -2 A$	THREED	2	.5	S			

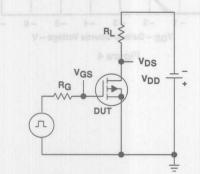
[†] Pulse test: pulse duration \leq 300 µs, duty cycle \leq 2%

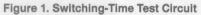
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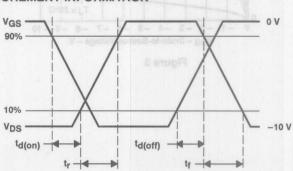
dynamic

	PARAMETER	Vin	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Qg	Total gate charge	Ba	V I I I I I I I I I I I I I I I I I I I	- = 80V	5.45		-	
Qgs	Gate-to-source charge	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, \qquad I_D = -1 \text{ A}$	$V_{DS} = -10 V$, $V_{GS} = -10 V$, $I_D = -1 A$ 0.87					nC
Qgd	Gate-to-drain charge			The	1.4	10		
td(on)	Turn-on delay time	1	43	- BOV	4.5		ns	
td(off)	Turn-off delay time	$V_{DD} = -10 V,$	$R_L = 10 \Omega$, $I_D = -1 A$, See Figures 1 and 2		13	8	ns	
tr	Rise time	R _G = 6 Ω,			10			
tf	Fall time	and and B			2		ns	
trr(SD)	Source-to-drain reverse recovery time	IF = 5.3 A,	di/dt = 100 A/µs		16			







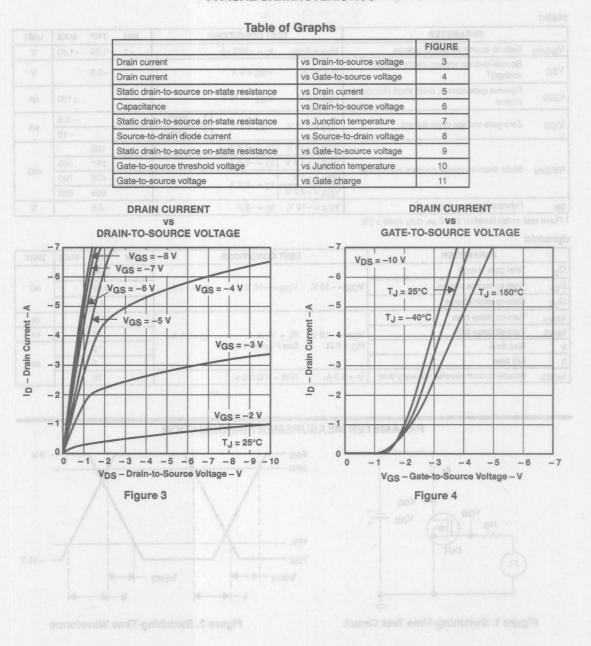






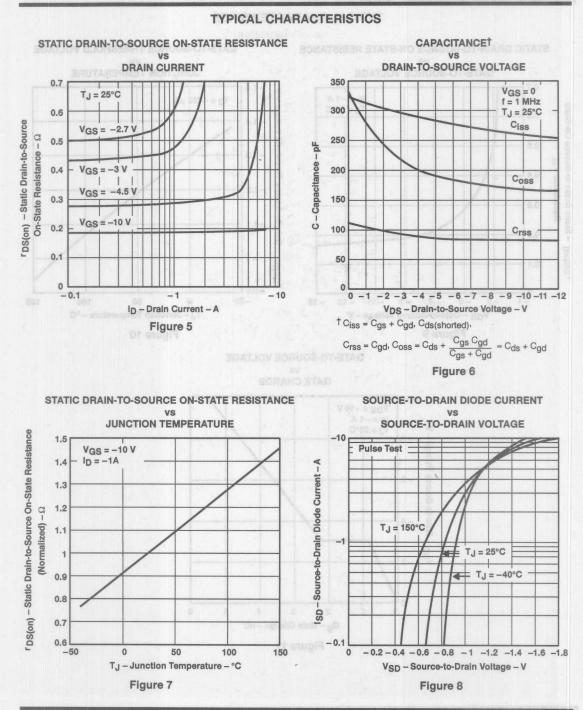
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TYPICAL CHARACTERISTICS



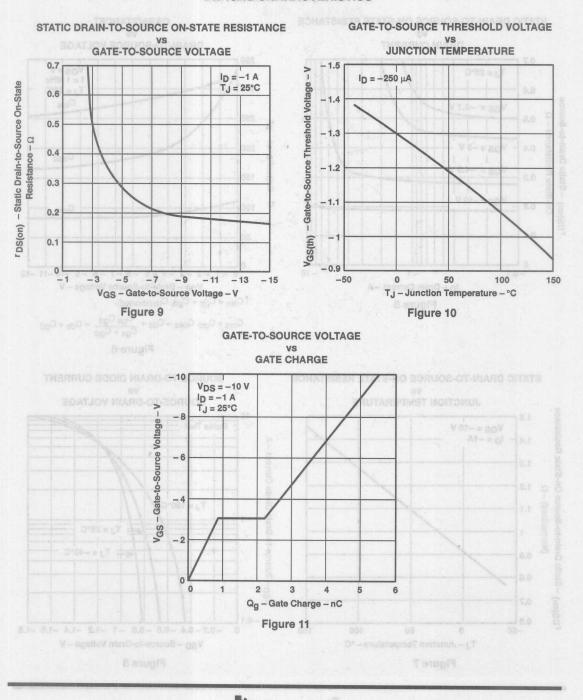


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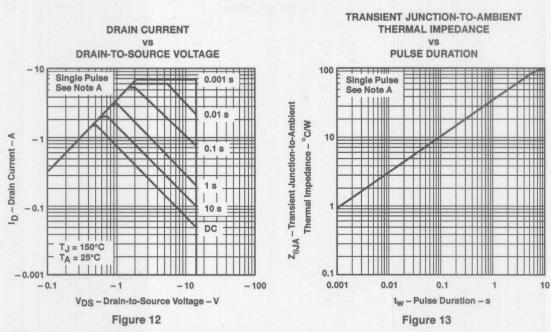
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TYPICAL CHARACTERISTICS

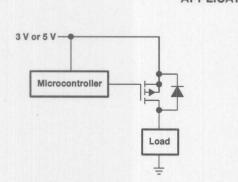


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THERMAL INFORMATION

NOTE A: Values are for the D package and are FR4-board mounted only.





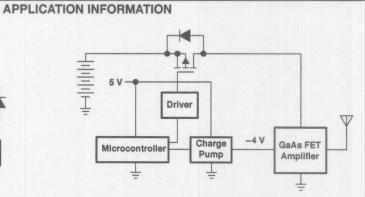


Figure 15. Cellular Phone Output Drive

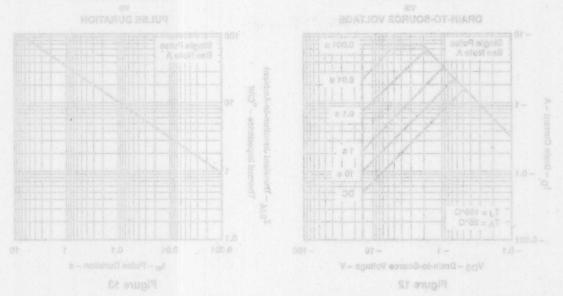


SINGLE P-CHANNEL ENHANCEMENT-MODE MOSPE

SLV8077A - DECEMBER 1003 - REVISED FEERING - ARTORVIS

NOTAMIAC INFORMATION





DTE A: Values are for the D package and are FR4-board mounted on

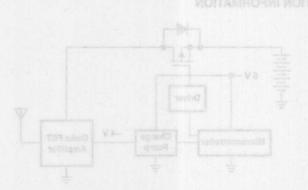
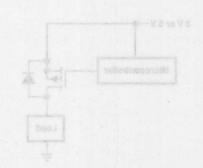


Figure 15, Cellular Phone Output Drive



Floure 14, Notebook Lood Management

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- Low r_{DS(on)}...0.09 Ω Typ at V_{GS} = -10 V
- 3-V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- V_{GS(th)} = -1.5 V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protected

description

The TPS1101 is a single, low- $r_{DS(on)}$, p-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOSTM process. With a maximum $V_{GS(th)}$ of -1.5 V and an I_{DSS} of only 0.5 μ A, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin TSSOP (PW) version fits in height-restricted places where other p-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an SOIC package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

AVAILABLE OPTIONS

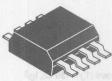
United Set	PACKAGED DEVICEST					
TJ	SMALL OUTLINE (D)	TSSOP (PW)				
-40°C to 150°C	TPS1101D	TPS1101PWLE				

[†] The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE).

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications par the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

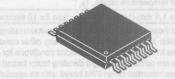
		T		
SOURCE	1	~	8] DRAIN
SOURCE [2		7] DRAIN
SOURCE	3		6	DRAIN
GATE	4		5	DRAIN



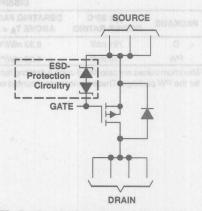
PW PACKAGE (TOP VIEW)

NC SOURCE SOURCE SOURCE SOURCE SOURCE SOURCE GATE NC SOURCE SOURC	10 16 2 15 3 14 4 13 5 12 6 11 7 10 8 9	NC DRAIN DRAIN DRAIN DRAIN DRAIN DRAIN DRAIN DRAIN
--	---	--

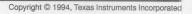
NC - No internal connection



schematic



NOTE: For all applications, all source pins should be connected and all drain pins should be connected.





				nadutor a	UNIT
Drain-to-source voltage, VDS		00	EXTRACTED V	- 15	V
Gate-to-source voltage, VGS	,	lbie Inputs	as Compai	2, - 15	V
SOURCE [& BRAIN			T _A = 25°C	±0.62	N B
	No. 071	D package	T _A = 125°C	±0.39	
	VGS = -2.7 V	-	T _A = 25°C	±0.61	
		PW package	T _A = 125°C	±0.38	
	V _{GS} = -3 V	Deselvere	T _A = 25°C	±0.88	
Continuous drain current (TJ = 150°C), ID [‡]		D package	T _A = 125°C	±0.47	199
		PW package	T _A = 25°C	±0.86	
			T _A = 125°C	±0.45	ed.
	V _{GS} = -4.5 V	D package	T _A = 25°C	±1.52	A
			T _A = 125°C	±0.71	
		PW package	T _A = 25°C	±1.44	
			T _A = 125°C	±0.67	
	Inter no Der	D package	T _A = 25°C	±2.30	
	V _{GS} = -10 V		T _A = 125°C	±1.04	
	VGS = - 10 V	PW package	T _A = 25°C	±2.18	
	epatiovea		T _A = 125°C	±0.98	97
Pulsed drain current, IDM [‡]	dohastor	NE TOWOG SE	ious enoites	±10	A
Continuous source current (diode conduction), IS	ollers or	NVM) contro	i) betaluba	-1.1	A
Storage temperature range, T _{stg}			.anevin	-55 to 150	°C
Operating junction temperature range, TJ	ni alih in	nolenev (WA	TSSOF (-40 to 150	°C
Operating free-air temperature range, TA	lennerlo-s	inera offici r	id places w	-40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	al snistr	evbe asta	nnol. The	260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

* Maximum values are calculated using a derating factor based on R_{0JA} = 158°C/W for the D package and R_{0JA} = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR [‡] ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/°C	454 mW	369 mW	142 mW

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 158^{\circ}C/W$ for the D package and $R_{\theta JA} = 176^{\circ}C/W$ for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

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electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT			
VGS(th)	Gate-to-source threshold voltage	V _{DS} = V _{GS} ,	l _D = -250 μA		-1	-1.25	-1.5	V			
VSD	Source-to-drain voltage (diode forward voltage)†	I _S = -1 A, V _{GS} = 0 V			sin Curve sin curve	-1.04		V			
IGSS	Reverse gate current, drain short circuited to source	V _{DS} = 0 V, V _{GS} = -12 V		niano olia	818	±100	nA				
la e e Zoro doto voltado droip ourropt	V 10.V	N 0.11	TJ = 25°C	ni soin, eite		-0.5					
IDSS	Zero-gate-voltage drain current	$V_{DS} = -12 V,$	$v_{DS} = -12 v,$	$v_{DS} = -12 v,$	$v_{DS} = -12 v$,	VGS = 0 V	TJ = 125°C	AL AM		-10	μA
	B what are a set of	VGS = -10 V	I _D = -2.5 A		stado effe	90					
		$V_{GS} = -4.5 V$	$I_{D} = -1.5 A$			134	190				
rDS(on)	Static drain-to-source on-state resistance†	$V_{GS} = -3 V$			ine	198	310 n	mΩ			
		VGS = -2.7 V	$I_{\rm D} = -0.5 {\rm A}$			232	400				
9fs	Forward transconductance [†]	$V_{DS} = -10 V,$	$I_D = -2 A$	THREAL	LARA!	4.3		S			

[†] Pulse test: pulse duration \leq 300 µs, duty cycle \leq 2%.

dynamic

PARAMETER		TEST CONDITIONS			MIN TYP	TYP	MAX	UNIT	
Qg	Total gate charge			V	and an and	11.25			
Qgs	Gate-to-source charge	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -1 A 1.5		$V_{S} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -1 \text{ A}$		1.5	8	nC	
Qgd	Gate-to-drain charge	1			VA-E	2.6			
td(on)	Turn-on delay time		VE	-= 80V	1	6.5		ns	
td(off)	Turn-off delay time	$V_{DD} = -10 V$,				19	1-18	ns	
tr	Rise time	R _G = 6 Ω,				5.5	11-10		
tf	Fall time					13		ns	
trr(SD)	Source-to-drain reverse recovery time	IF = 5.3 A,	di/dt = 100 A/µs			16			

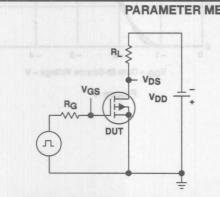


Figure 1. Switching-Time Test Circuit

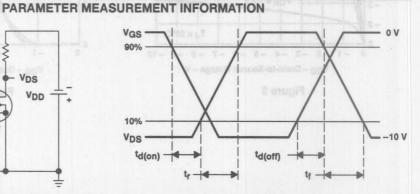


Figure 2. Switching-Time Waveforms

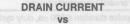


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TYPICAL CHARACTERISTICS

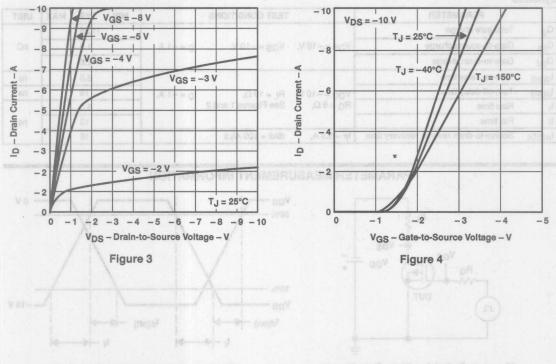
	INT NIM BHOLTICH US IS	of Graphs	RETER	9	
	10 =250 uA	ollage Vos-Vos-	FIGURE	Gate-to-ebu	
	Drain current	vs Drain-to-source voltage	3	Source-to-th	
	Drain current	vs Gate-to-source voltage	4	T(epsiloy	
	Static drain-to-source on-state resistance	vs Drain current	5	Reverso get	
	Capacitance	vs Drain-to-source voltage	6	Boilloa	
-0.5	Static drain-to-source on-state resistance	vs Junction temperature	onia 7 angli	Zaro-gale-vi	
	Source-to-drain diode current	vs Source-to-drain voltage	8		
-	Static drain-to-source on-state resistance	vs Gate-to-source voltage	9		
	Gate-to-source threshold voltage	vs Junction temperature	10	Stallo disin-	
	Gate-to-source voltage	vs Gate charge	11		

DRAIN CURRENT vs



DRAIN-TO-SOURCE VOLTAGE

GATE-TO-SOURCE VOLTAGE

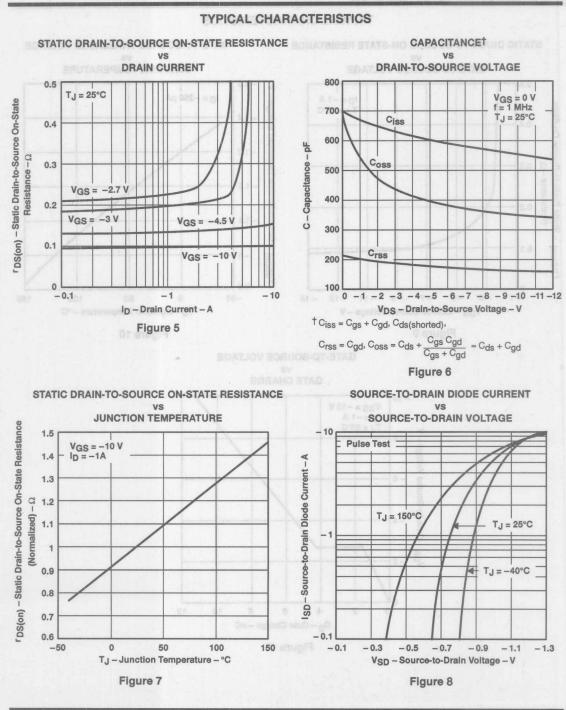


titre 1. Switching Time Test Circuit



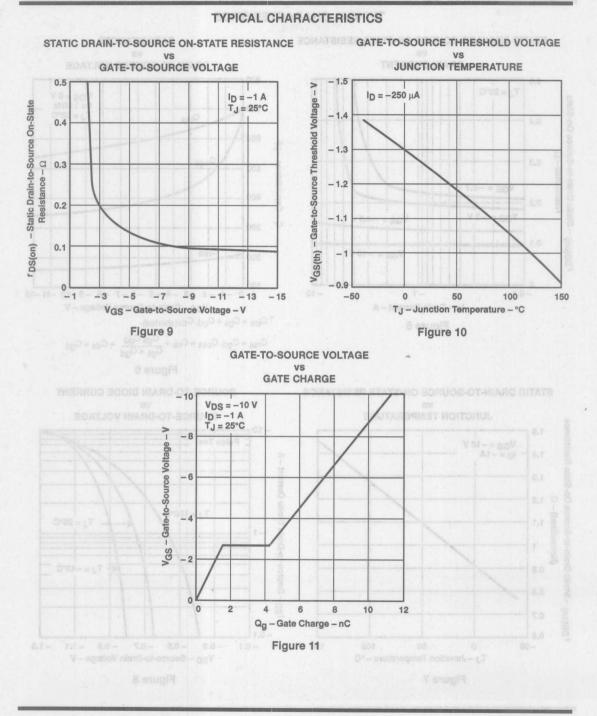
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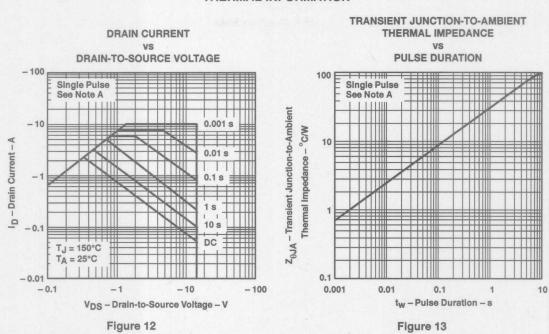


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THERMAL INFORMATION

NOTE A: Values are for the D package and are FR4-board-mounted only.

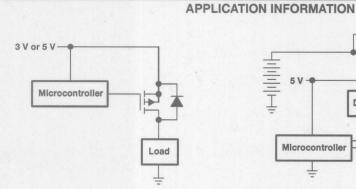


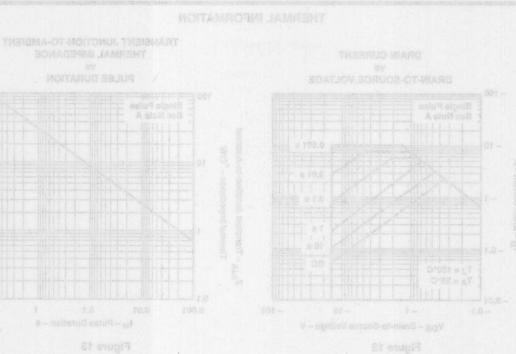
Figure 14. Notebook Load Management

Figure 15. Cellular Phone Output Drive

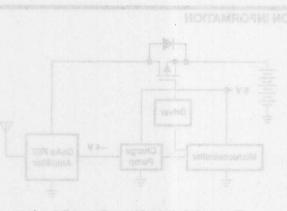




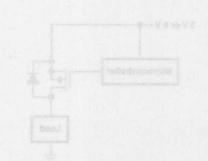




IOTE A: Values are for the D package and are FR4-board-mounted only.



Floure 15. Cellular Phone Output Drive



Floure 14, Notebook Loud Management

General Information	1
Operational Amplifiers	2
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Analog-to-Digital Converters	6
Line Driver/Receiver	7
Mechanical Data	8



TLV1543C, TLV1543M 3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS SLAS072A - DECEMBER 1992 - REVISED DECEMBER 1993

● Advanced LinEPIC [™] Technology	DW, FK, J, OR N PACKAGE	
3.3-V Supply Operation	(TOP VIEW)	
• 10-Bit-Resolution A/D Converter		
11 Analog Input Channels		
Three Built-In Self-Test Modes	A2 3 18 1/O CLOC	ĸ
Inherent Sample and Hold	A3 4 17 ADDRES	S
Total Unadjusted Error ±1 LSB Max	A4 🛛 5 16 🗋 DATA OU	T
On-Chip System Clock	A5 6 15 CS	0.0
	A6 7 14 REF+	
End-of-Conversion (EOC) Output	A7 🛛 8 13 🗍 REF-	
Pin Compatible With TLC1543	A8 9 12 A10	
description	GND [10 11] A9	

The TLV1543C and TLV1543M are Advanced LinEPIC[™] 10-bit, switched-capacitor, successive-approximation, analog-to-digital converters. These devices have three inputs and a 3-state output [chip select (CS), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct four-wire interface to the serial port of a host processor. The devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLV1543C is characterized for operation from 0°C to 70°C. The TLV1543M is characterized for operation over the full military temperature range of -55°C to 125°C.

1	PACKAGED DEVICES					
TA	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)		
0°C to 70°C	TLV1543CDW		-	TLV1543CN		
-55°C to 125°C	-	TLV1543MFK	TLV1543MJ	_		

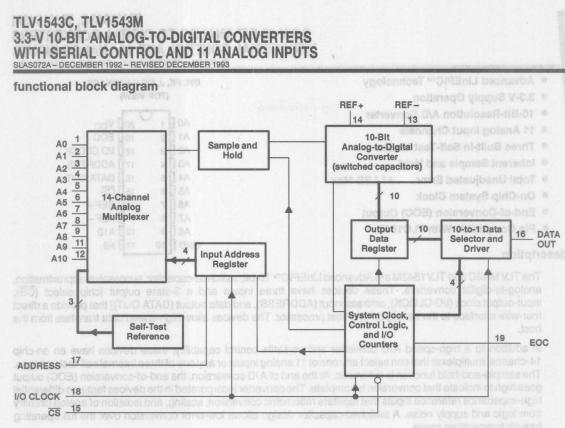
AVAILABLE OPTIONS

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Ine FLV1543C is characterized for operation from 0°C to 70°C. The TLV1543M is characterized for operation over the full military temperature range of –55°C to 125°C.

озельно bip (4)	CHIP CARNER (FR)	
LIMENATVIT		

dvanced UnEPIC is a trademark of Texts Instruments it



TLV1543C, TLV1543M 3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS SLAS072A - DECEMBER 1992 - REVISED DECEMBER 1993

Terminal Functions

TI NAME	ERMINAL E NO.	1/0	DESCRIPTION
ADDRES	58 17 17 17 19 10 10 10 10 10 10 10 10 10 10 10 10 10	ettor 85 þ suga	Serial address. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.
A0-A10	1–9, 11, 12	T	Analog signal. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 k Ω .
CS	n mcets 1, mede failing edge in n C. Ten bits of d	105 000 1000	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OU	JT 16 Juga and bas a Juga and bas a Juga and bas Juga and bas Juga and bas	NON NON TUO NON	The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when \overline{CS} is high and active when \overline{CS} is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	0	End of conversion. This output goes from a high- to a low- logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	1	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOO	CK 18 Complete Cronget Tronget Stonget		 Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	12	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF – terminal.
REF-	13	1	The lower reference voltage value (nominally ground) is applied to this terminal.
Vcc	20	1	Positive supply voltage

detailed description

With chip select (\overline{CS}) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes \overline{CS} active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host. The first four I/O clocks load the address register with the 4-bit address on ADDRESS selecting the desired analog channel and the next six clocks providing the control timing for sampling the analog input.

In this thoos, Us is active (low) perween senal I/O CLOCK transfers and each transfer is terricorie long, At the initial conversion cycle, C3 is held active (low) for subsequent conversions; the rising adge of EOC the begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previo



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detailed description (continued)

NH Kerstrater

There are six basic serial interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of \overline{CS} as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and \overline{CS} inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and \overline{CS} active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between conversion cycles, (4) a fast mode with a 16-bit transfer and \overline{CS} active (low) continuously, (5) a slow mode with a n 11- to 16-clock transfer and \overline{CS} inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and \overline{CS} active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of \overline{CS} in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the 16th clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the 10th clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. On the 10th clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of \overline{CS} , the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

MODES		CS	NO. OF I/O CLOCKS	MSB AT DATA OUT	TIMING
	Mode 1	High between conversion cycles	10	CS falling edge	Figure 9
igbe gnich tuo Feet Medee	Mode 2	Low continuously	10	EOC rising edge	Figure 10
Fast Modes	Mode 3	High between conversion cycles	11 to 16 [‡]	CS falling edge	Figure 11
	Mode 4	Low continuously	16‡	EOC rising edge	Figure 12
Oleve Medee	Mode 5	High between conversion cycles	11 to 16‡	CS falling edge	Figure 13
Slow Modes	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 14

Table 1. Mode Operation

[†]These edges also initiate serial interface communication.

[‡]No more than 16 clocks should be used.

fast modes

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the 10th I/O CLOCK.

mode 1: fast mode, CS inactive (high) between conversion cycles, 10-clock transfer

In this mode, CS is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of CS begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of CS ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of CS disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, CS active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.



mode 3: fast mode, CS inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, CS active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

slow modes

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the 11th clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host serial interface, and \overline{CS} has to be toggled to initialize the system. The 11th rising edge of the I/O CLOCK must occur within 9.5 µs after the 10th I/O clock falling edge.

mode 5: slow mode, CS inactive (high) between conversion cycles, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, CS active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the 16th I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

address bits

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or 3 internal test inputs).

analog inputs and test modes

The 11 analog inputs and the 3 internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the 10th I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

capacitor remains connected to REF + through the remainder of the successive-approximation process, process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line un bits are consisted.



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6-clock transfer

Table 2. An	alog-Channel-Select Address	
-------------	-----------------------------	--

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT		
SELECTED	BINARY	HEX	
AO	0000	0	
A1	0001	1	
A2	0010	2 0	
A3	0011	3	
A4	0100	30 4	
A5	0101	5	
A6	0110	6	
A7	0111	. 7	
A8	1000	8	
A9	1001	9	
A10	1010	A	

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE	VALUE SHIFT ADDRESS	ED INTO	OUTPUT RESULT (HEX)‡
SELECTED	BINARY	HEX	Is the sequence by retur
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	В	200
V _{ref} -	1100	С	000
V _{ref+}	1101	D	3FF

[†] V_{ref+} is the voltage applied to the REF + input, and V_{ref} is the voltage applied to the REF input.

[‡] The output results shown are the ideal values and vary with the reference stability and with and the set of the set

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all ST and SC switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.



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converter and analog input (continued)

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

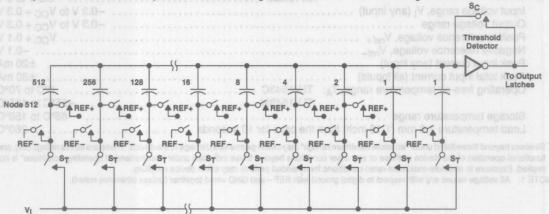


Figure 1. Simplified Model of the Successive-Approximation System

chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent \overline{CS} from being taken low close to completion of conversion because the output data can be corrupted.

reference voltage inputs

There are two reference inputs used with these devices: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} (see Note 1): TLV1543C
Input voltage range, V _I (any input)0.3 V to V _{CC} + 0.3 V
Output voltage range
Negative reference voltage, V _{ref}
Peak input current (any input) ±20 mA
Peak total input current (all inputs)
TLV1543M
Storage temperature range

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).

Figure 1. Simplified Model of the Successive-Approximation System

10051000 100108-0010

The trailing edge of CS starts all modes of operation, and CS can abort a conversion sequence in any mode, A high-to-low transition on CS within the spacified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent CS from being taken low close to completion of conversion because the output data can be conversion exclusion.

reference voltage inputs

There are two reference inputs used with these devices: REF + and REF -. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF +, REF -, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF + and at zero when the input signal is equal to or lower than REF -.



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Property and and	FIOT STILL T	a Youanbau whome	MIN	NOM	MAX	UNI	
Supply voltage, V _{CC}	TLV1543C		3	3.3	5.5	V	
	TLV1543M		3	3.3	3.6	V	
Positive reference voltage, Vref+ (see Note 2)	Ave 6.1 Real	V 8 × ooV		Vcc		V	
Negative reference voltage, Vref- (see Note 2)	Au 0S = HOI	V 8.8 at V 8 = 33V	Coedi vy	0	tuo laval-rtol)-	V	
Differential reference voltage, Vref+ - Vref- (see	Note 2)	V Excav	2.5	VCC	V _{CC} +0.2	V	
Analog input voltage (see Note 2)	Au 08 = Hot	Ven #3 V to 3.6 V.	0		Vcc	V	
High-level control input voltage, VIH	TLV1543C	V _{CC} = 3 V to 5.5 V	2			V	
	TLV1543M	V _{CC} = 3 V to 3.6 V	2	the second	inveleval out	V	
Low-level control input voltage, VIL	TLV1543C	V _{CC} = 3 V to 5.5 V			0.6	V	
	TLV1543M	V _{CC} = 3 V to 3.6 V	N GROINS		0.8	V	
Setup time, address bits at data input before I/O CLOCK1, tsu(A)			100	bisomi-	user energy BC	ns	
Hold time, address bits after I/O CLOCK [↑] , t _{h(A)}		0		Inimus fuglur	ns		
Hold time, CS low after last I/O CLOCK↓, th(CS)			0	ut currer	ork level-dbli	ns	
Setup time, CS low before clocking in first addres	s bit, t _{su(CS)} (see N	Note 3)	1.425	a curren	rgni level-wo.	μs	
am 130	TLC1543C		0	muo via	1.1	MHz	
Clock frequency at I/O CLOCK (see Note 4)	TLC1543M		0		2.1		
Pulse duration, I/O CLOCK high, t _{wH(I/O)}			190	10757 1791.0	water conversion	ns	
Pulse duration, I/O CLOCK low, twL(I/O)			190	olaria di	ate mumbrak	ns	
Transition time, I/O CLOCK, tt(I/O) (see Note 5)				+ 12	1	μs	
Transition time, ADDRESS and CS, tt(CS)			C ENATV3	,ecn	elosq 10 qr	μs	
Operating free-air temperature, TA	TLV1543C		0	1	70	°C	
Operating nee-an temperature, 1A	TLV1543M		-55	· .eon	125	C	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111), while input voltages less than that applied to REF- convert as all zeros (000000000). The device is functional with reference voltages down to 1 V (Vref+ - Vref-); however, the electrical specifications are no longer applicable.

3. To minimize errors caused by noise at CS, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after CSJ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum CS setup time has elapsed.

4. For 11- to 16-bit transfers, after the 10th I/O CLOCK falling edge (≤ 2 V), at least 1 I/O clock rising edge (≥ 2 V) must occur within 9.5 µs.

5. This is the time required for the clock input signal to fall from VIHmin to VILmax or to rise from VILmax to VIHmin. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 3 V$ to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+} = 3 V$ to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYPT	MAX	UNIT		
Vон	High-level output voltage	TLV1543C	V _{CC} = 3 V,	I _{OH} = -1.6 mA	2.4	equiliov e	onana)o	V	
			V _{CC} = 3 V to 5.5 V,	I _{OH} = 20 μA	V _{CC} -0.1	affry eu	(1016) 61	V	
		TLV1543M	V _{CC} = 3 V,	I _{OH} = -1.6 mA	2.4	sellov eoo	al ratera	V	
			V _{CC} = 3 V to 3.6 V,	l _{OH} = 20 μA	Vcc-0.1	1.000) ağa	diav jug	V	
VOL	Low-level output voltage	TLV1543C	V _{CC} = 3 V,	I _{OL} = 1.6 mA	and and	tion through	0.4	V	
			V _{CC} = 3 V to 5.5 V,	IOL = 20 μA			0.1	V	
		TLV1543M	V _{CC} = 3 V,	IOL = 1.6 mA	ist who	day provi	0.4	V	
			V _{CC} = 3 V to 3.6 V,	l _{OL} = 20 μA			0.1	V	
loz	Off-state (high-impedance-state) output current		$V_{O} = V_{CC},$	CS at V _{CC}	d luqui intab	tis effol ales	10	μА	
			V _O = 0,	CS at V _{CC}	100.10 OV X	alls alid a	-10		
ΙΗ	High-level input current		VI = VCC	(80)d -	100 10 0/1	0.005	2.5	μA	
IL SA	Low-level input current		VI = 0 (Source) (Source) (Source) and source a		a ni grabloate	-0.005	-2.5	μA	
ICC	Operating supply current		CS at 0 V	TLOIS AND	All man line	0.8	2.5	mA	
	Selected channel leakage current		Selected channel at V _{CC} , Unselected channel at 0 V				1		
			Selected channel at 0 V, Unselected channel at V _{CC}		High whith	0.01000	-1	μA	
an Ru	Maximum static analog reference current into REF +		V _{ref+} = V _{CC} ,	V _{ref-} = GND	()(), (w), (w()) (1000), (1000), (1000)	0 61.00K	10	μA	
Ci	Input capacitance, Analog inputs	TLV1543C		12	and CS, the	7	55	00.F	
		TLV1543M		TT.V1843C		7		pF	
	Input capacitance, Control inputs	TLV1543C		TREASING	W. C. Norman	5	15	pF	
		TLV1543M	THEFT PART IS AN TA	and a REPART of her loan texts again the	almo sacredo	5	A A		

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

the electrical epecifications are no longer applicable

To minimus errore caused by holes at \overline{CS} , the Internal cliculity waits for a setup time that two falling edges of the internal system diotic after \overline{CS} . before exerciceling to control input signuls. Therefore, no straings enould be marks to clock in an address grint the minimum \overline{CS} actus time has eliticaed.

For 11- to 16-bit transitive, where the 10th UO OLCOCK with a edge (2.2 V), at least 1.00 clock rising edge (2.2 V) must eccur within 9.5 ps.

This is the time required for the abolic right signal to fail from Vigenic to Vigenes or to the from Vigenes to Vigenic. In the violity of normal from temperature, the devices function with input one of the mattern time as select as 1 to for mende data, eacy stiftion applications.

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operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 3 V$ to 5.5 V, I/O CLOCK frequency = 1.1 MHz for the TLV1543C, $V_{CC} = V_{ref+} = 3 V$ to 3.6 V, I/O CLOCK frequency = 2.1 MHz for the TLV1543M

	PARAMETER	TEST CONDITIONS	MIN	TYPT	MAX	UNIT
	Linearity error (see Note 6)				±1	LSB
	Zero error (see Note 7)	See Note 2		Commission of	±1	LSB
	Full-scale error (see Note 7)	See Note 2			±1,	LSB
	Total unadjusted error (see Note 8)	S 12 802 M	12	1 49 08	±1	LSB
		ADDRESS = 1011		512		
	Self-test output code (see Table 3 and Note 9)	ADDRESS = 1100		0		1
		ADDRESS = 1101		1023		1
tconv	Conversion time	See timing diagrams			21	μs
tc	Total cycle time (access, sample, and conversion)	See timing diagrams and Note 10			21 +10 I/O CLOCK periods	μs
tacq	Channel acquisition time (sample)	See timing diagrams and Note 10	1		6	I/O CLOCK periods
tv	Valid time, DATA OUT remains valid after I/O CLOCK	See Figure 6	10	1		ns
td(I/O-DATA)	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6		EVAS	240	ns
td(I/O-EOC)	Delay time, 10th I/O CLOCK↓ to EOC↓	See Figure 7		70	240	ns
td(EOC-DATA)	Delay time, EOCT to DATA OUT (MSB)	See Figure 8			100	ns
tPZH, tPZL	Enable time, CSJ to DATA OUT (MSB driven)	See Figure 3	24134 0	1100	1.3	μs
tPHZ, tPLZ	Disable time, CST to DATA OUT (high impedance)	See Figure 3			150	ns
tr(EOC)	Rise time, EOC	See Figure 8			300	ns
tf(EOC)	Fall time, EOC	See Figure 7			300	ns
tr(bus)	Rise time, data bus	See Figure 6			300	ns
tf(bus)	Fall time, data bus	See Figure 6			300	ns
td(I/O-CS)	Delay time, 10th I/O CLOCK \downarrow to $\overline{CS} \downarrow$ to abort conversion (see Note 11)		2003	2.01	9	μs

[†] All typical values are at $T_A = 25^{\circ}C$.

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (111111111), while input voltages less than that applied to REF – convert as all zeros (000000000). The device is functional with reference voltages down to 1 V (V_{ref+} – V_{ref-}); however, the electrical specifications are no longer applicable.

6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

 Zero error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.

8. Total unadjusted error comprises linearity, zero, and full-scale errors.

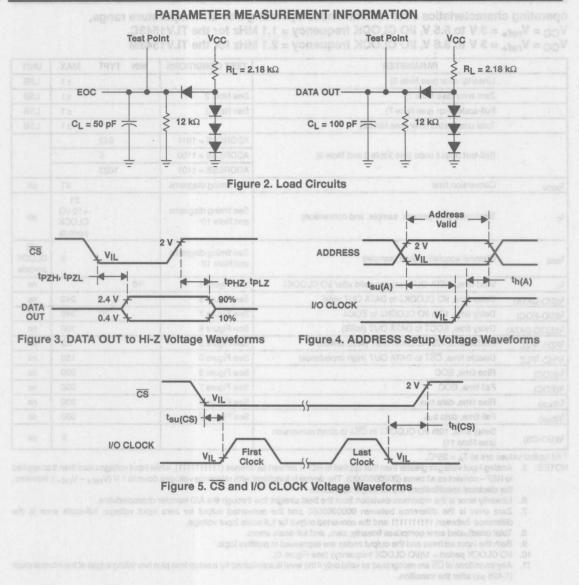
9. Both the input address and the output codes are expressed in positive logic.

10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6).

 Any transitions of CS are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 μs) after the transition.

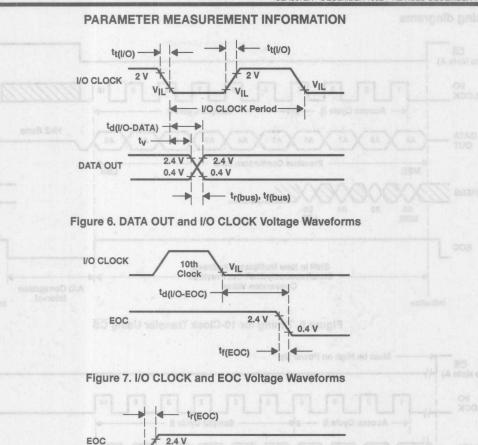


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td(EOC-DATA)

DATA OUT

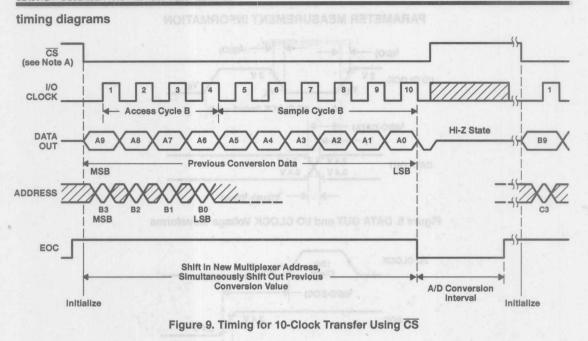
0.4 V

laure 10. Tantag for 10-Clock Transfer Not Using C

ADTE A: "To minimize encessed by noise it US, the internal directing with for a solup time plot two facing adges of the internal system cloc inter USL before responding to control input highests. Provenue, no attempt should be made to deck to an address until the minimu



TLV1543C, TLV1543M 3.3-V 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS SLAS072A – DECEMBER 1992 – REVISED DECEMBER 1993



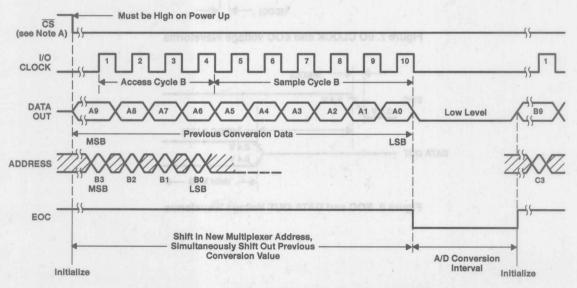
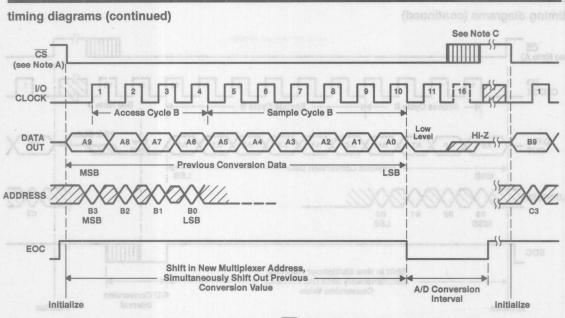


Figure 10. Timing for 10-Clock Transfer Not Using CS

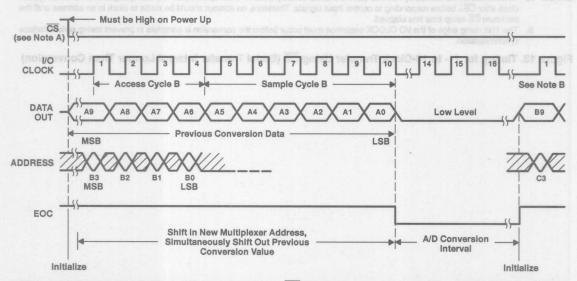
NOTE A: To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS} \downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.



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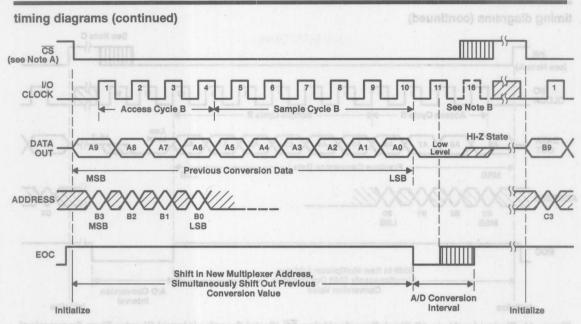




- NOTES: A. To minimize errors caused by noise at CS, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after CSJ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum CS setup time has elapsed.
 - B. The first I/O CLOCK must occur after the rising edge of EOC.
 - C. A low-to-high transition of CS disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.



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NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a set up time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum \overline{CS} setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

Figure 13. Timing for 11- to 16-Clock Transfer Using CS (Serial Transfer Interval Longer Than Conversion)

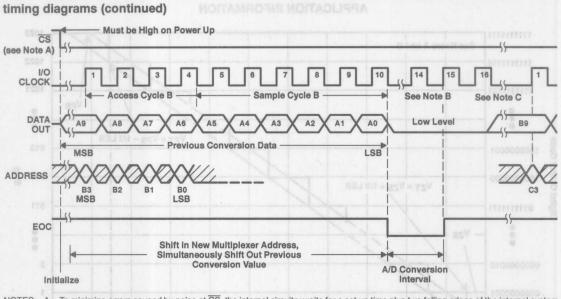


- KOTES: A. To minimize errors caused by noise at US, the internet circulary write for a set to firm plus two fulling edges of the interdat system clock after OSU before responding to control input signals. Therefore, no etimol the made to clock in an address until the minimum US setup time hos elegand.
 - B. The first UO CLOCK must occur after the sistin edn
- A power-hear researce of CS deather ADDRESS and the I/O CLOCK within a castraum of a setue time of us failing address of
 - the manual system matrix lands and



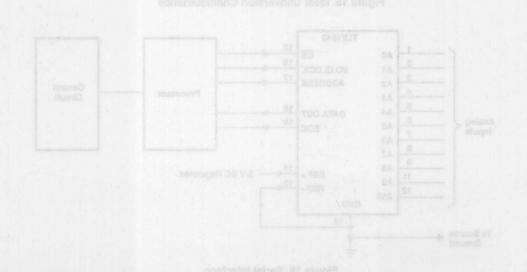
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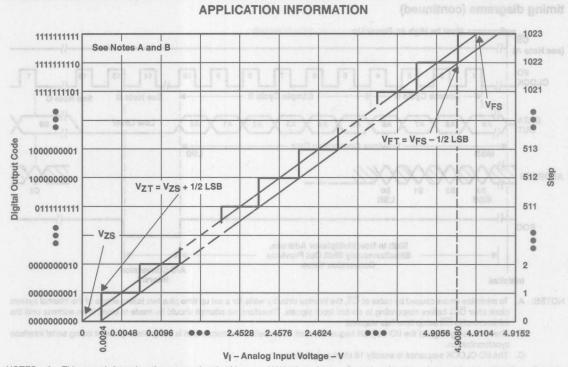
- NOTES: A. To minimize errors caused by noise at CS, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after CS1 before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum chip CS setup time has elapsed.
 - B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.
 - C. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using CS (Serial Transfer Interval Longer Than Conversion)





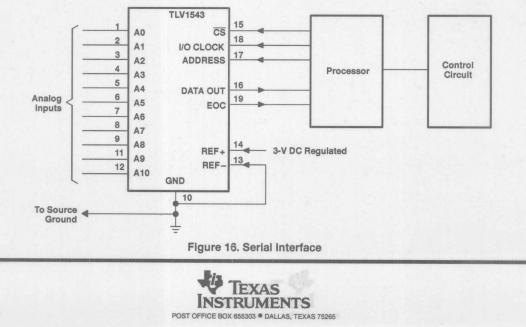
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NOTES: A. This curve is based on the assumption that V_{ref} + and V_{ref} + have been adjusted so that the voltage at the transition from digital 0 to 1 (V_ZT) is 0.0024 V and the transition to full scale (V_FT) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

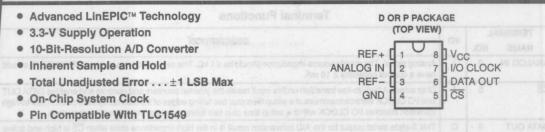




6-20

TLV1549C **10-BIT ANALOG-TO-DIGITAL CONVERTER** WITH SERIAL CONTROL





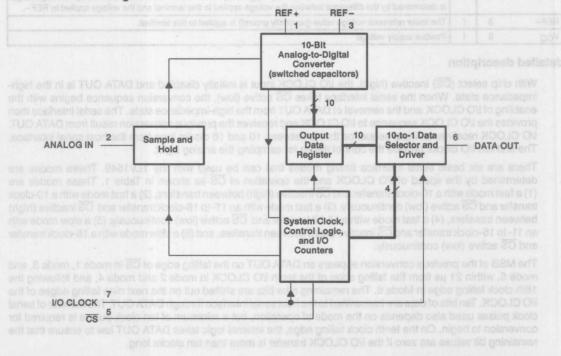
description

The TLV1549C is a 10-bit, switched-capacitor, successive-approximation analog-to-digital converter. The device has two digital inputs and a 3-state output [chip select (CS), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

The sample-and-hold function is automatic. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLV1549C is characterized for operation from 0°C to 70°C.

functional block diagram



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			Terminal Functions
TERMINAL NAME	NO.	1/0	DESCRIPTION
ANALOG IN	2	oli	Analog signal. The driving source impedance should be $\leq 1 \text{ k}\Omega$. The external driving source to ANALOG IN should have a current capability $\geq 10 \text{ mA}$.
CS	5	a5 [Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT			This 3-state serial output for the A/D conversion result is in the high-impedance state when \overline{CS} is high and active when \overline{CS} is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4	oi lec noite	The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	7	1910	 The input/output clock receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	-1	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to REF
REF-	3	1	The lower reference voltage value (nominally ground) is applied to this terminal.
Vcc	8	1	Positive supply voltage

detailed description

With chip select (CS) inactive (high), the I/O CLOCK input is initially disabled and DATA OUT is in the highimpedance state. When the serial interface takes CS active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLV1549. These modes are determined by the speed of I/O CLOCK and the operation of \overline{CS} as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and \overline{CS} inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and \overline{CS} inactive (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and \overline{CS} active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and \overline{CS} inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and \overline{CS} active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of \overline{CS} in mode 1, mode 3, and mode 5, within 21 µs from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the 16th clock falling edge in Mode 6. The remaining nine bits are shifted out on the next nine falling edges of the I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

NSTRUMENTS

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detailed description (continued)

Table 1 lists the operational modes with respect to the state of \overline{CS} , the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.

MODES		MODES doin or most TUO A CS antivories		MSB AT DATA OUT	TIMING DIAGRAI	
r ter tr chi thiw a	Mode 1	High between conversion cycles	10	CS falling edge	Figure 6	
East Mades	Mode 2	Low continuously	10	Within 21 µs	Figure 7	
Fast Modes	Mode 3	High between conversion cycles	11 to 16‡	CS falling edge	Figure 8	
	Mode 4	Low continuously	16‡	Within 21 µs	Figure 9	
Church and	Mode 5	High between conversion cycles	11 to 16‡	CS falling edge	Figure 10	
Slow Modes	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11	

		Table	11	Mode	0	peration
--	--	-------	----	------	---	----------

[†]This timing also initiates serial interface communication.

‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21 μ s after the falling edge of the 10th I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer, \overline{CS} must be active (low) so that the I/O CLOCK input is enabled. When \overline{CS} is toggled between data transfers (modes 1, 3, and 5), the transitions at \overline{CS} are recognized as valid only if the level is maintained for a minimum period of 1.425 μ s after the transition. If the transfer is more than 10 I/O clocks (modes 3, 4, 5, and 6), the rising edge of the 11th clock must occur within 9.5 μ s after the falling edge of the 10th I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and \overline{CS} has to be toggled to restore proper operation.

fast modes of tent end of the

The device is in a fast mode when the serial I/O CLOCK data transfer is completed within 21 µs from the falling edge of the tenth I/O CLOCK. With a 10-clock serial transfer, the device can only run in a fast mode.

mode 1: fast mode, CS inactive (high) between transfers, 10-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O-CLOCK transfers, and each transfer is ten clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 2: fast mode, CS active (low) continuously, 10-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O-CLOCK transfers and each transfer is 10 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the 10th I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

mode 3: fast mode, CS inactive (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is inactive (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 4: fast mode, CS active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. Within 21 μ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.



slow modes

permituos) tionduoiseo pemeteo

In a slow mode, the serial I/O CLOCK data transfer is completed after 21 µs from the falling edge of the 10th I/O CLOCK.

mode 5: slow mode, CS active (high) between transfers, 11- to 16-clock transfer

In this mode, \overline{CS} is active (high) between serial I/O-CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of \overline{CS} begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of \overline{CS} ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of \overline{CS} disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

mode 6: slow mode, CS active (low) continuously, 16-clock transfer

In this mode, \overline{CS} is active (low) between serial I/O-CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, \overline{CS} is held active (low) for subsequent conversions. The falling edge of the 16th I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

analog input sampling as ad team 20 releases tabk XOO JO OV takes a galved may econoupee releases

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

converter and analog input blues solves and service (COCJO OU do)t and to egbs guills

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

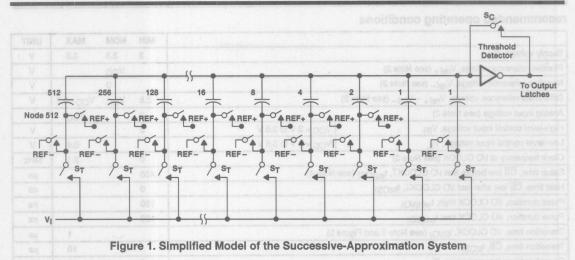
In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

iong. The tailing edge of CS begins the sequence by removing DATA OUT from the high-impedunce state. T rising edge of CS ends the sequence by returning DATA OUT to the high-impedance state within the specifi delay time. Also, the rising edge of CS disables VG CLOCK within a setup time plus two falling edges of the internal system otock.

In this mode, CS is active (low) between sarial I/O-CLOCK transfers and each transfer must be exactly 16 clocks for this mode, CS is active (low) between sarial I/O-CLOCK transfers and each transfer must be exactly 16 clocks forg. After the initial conversion cycle, CS is held active (low) for subsequent conversions. Within 21 µs aller the falling edge of the tenth I/O CLOCK, the MSR of the previous conversion appears at CATA OUT.





chip-select operation

The trailing edge of \overline{CS} starts all modes of operation, and \overline{CS} can abort a conversion sequence in any mode. A high-to-low transition on \overline{CS} within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent \overline{CS} from being taken low close to completion of conversion because the output data may be corrupted.

reference voltage inputs

There are two reference inputs used with the TLV1549: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading, respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} (see Note 1)
Input voltage range, V _I (any input) -0.3 V to V _{CC} + 0.3 V
Output voltage range
Positive reference voltage, V _{ref+}
Negative reference voltage, V _{ref-}
Peak input current (any input) ±20 mA
Peak total input current (all inputs)
Operating free-air temperature range, T _A
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF- and GND wired together (unless otherwise noted).



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, VCC		3	3.3	3.6	V
Positive reference voltage, Vref+ (see Note 2)			Vcc		V
Negative reference voltage, Vref- (see Note 2)			0		V
Differential reference voltage, Vref+ - Vref- (se	2.5	Vcc	V _{CC} +0.2	V	
Analog input voltage (see Note 2)	A ners - Caners - Caners - Caners - Ca	0	0-1.	Vcc	V
High-level control input voltage, VIH	V _{CC} = 3 V to 3.6 V	2		9-1	V
Low-level control input voltage, VIL	V _{CC} = 3 V to 3.6 V	497	14	0.6	V
Clock frequency at I/O CLOCK (see Note 3)				2.1	MHz
Setup time, CS low before first I/O CLOCK1, tsu	u(CS) (see Note 4)	1.425	The N	and a start	μs
Hold time, CS low after last I/O CLOCK↓, th(CS))	0			ns
Pulse duration, I/O CLOCK high, twH(I/O)		190			ns
Pulse duration, I/O CLOCK low, twL(I/O)	branch branch branch bran from	190	- Jammer		ns
Transition time, I/O CLOCK, tt(I/O) (see Note 5			1	μs	
Transition time, CS, tt(CS)	billied Model of the Successive-Appro	mila it a	mbid.	10	μs
Operating free-air temperature, TA		0	mak	70	°C

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (111111111), while input voltages less than that applied to REF - convert as all zeros (000000000). The TLV1549 is functional with reference voltages down to 1 V (V_{ref +} - V_{ref}-); however, the electrical specifications are no longer applicable.

 For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V), at least one I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 μs.

4. To minimize errors caused by noise at CS, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after CS ↓ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum CS setup time has elapsed.

5. This is the time required for the clock input signal to fall from V_Iµmin to V_Iµmax or to rise from V_Iµmax to V_Iµmin. In the vicinity of normal room temperature, the device functions with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 3 V$ to 3.6 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	MIN	TYPT	MAX	UNIT	
VOH High-level output voltage		1	V _{CC} = 3 V, I _{OH} = -1.6 m/		2.4			V	
			V _{CC} = 3 V to 3.6 V,	IOH = -20 μA	V _{CC} -0.1	muterity	1000 0	V	
Voi	Low-level output voltage		V _{CC} = 3 V,	I _{OL} = 1.6 mA			0.4		
VOL	Low-level output voltage		V _{CC} = 3 V to 3.6 V,	I _{OL} = 20 μA	anga, Voo	60161	0.1	usv.	
IOZ Off-state (high-impedance-state) output current		$V_{O} = V_{CC},$	CS at V _{CC}	Kurel IA 'sillin	12.1 GPs	10	3111		
		e) output current	V _O = 0,	CS at V _{CC}	A A A A A A A A A A A A A A A A A A A	Corgani	-10	μA	
ΠΗ	High-level input current		VI = VCC		anotos and	0.005	2.5	μΑ	
ΙIL	Low-level input current		VI = 0	A STATE	cont yout tool	0.005	-2.5	μA	
ICC	Operating supply current		CS at 0 V		climent (alt	0.4	2.5	mA	
70°C	Applog input lookago ourropt		VI = VCC	re range, TA	air temperat.	1-00 ⁺	0111	QQ	
S0°C	Analog input leakage current		VI == 0	Section Contraction of the	abuta range	redute	-1	μA	
9°08	Maximum static analog referen REF+	V _{ref+} = V _{CC} ,	V _{ref} = GND) nen dut en	STERES Standard	10	μА		
C.	logut especitores	Analog input	During sample cycle	ia er any other oot	e device at the	30	55	notor	
Ci	Input capacitance Control inputs		In ziones becomber	ol pupilipuco pistes	PLAN KARY KOUND	5	15	pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



operating characteristics	over recommended operating free-air temperature range,	
$V_{CC} = V_{ref+} = 3 V to 3.6 V,$	I/O CLOCK frequency = 2.1 MHz	

	PARAMETER	TEST CONDITIONS	MIN MAX	UNIT
	Linearity error (see Note 6)		±1	LSB
	Zero error (see Note 7)	See Note 2	±1	LSB
	Full-scale error (see Note 7)	See Note 2	±1	LSB
	Total unadjusted error (see Note 8)		±1	LSB
tconv	Conversion time	See timing diagrams	21	μs
tc	Total cycle time (access, sample, and conversion)	See timing diagrams and Note 9	21 +10 I/O CLOCK periods	μs
t _v	Valid time, DATA OUT remains valid after I/O CLOCK	See Figure 5	10	ns
td(I/O-DATA)	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 5	240	ns
tPZH, tPZL	Enable time, CS↓ to DATA OUT (MSB driven)	See Figure 3	1.3	μs
tPHZ, tPLZ	Disable time, CST to DATA OUT (high impedance)	See Figure 3	180	ns
t _{r(bus)}	Rise time, data bus	See Figure 5	300	ns
tf(bus)	Fall time, data bus	See Figure 5	300	ns
td(I/O-CS)	Delay time, 10th I/O CLOCK \downarrow to $\overline{CS} \downarrow$ to abort conversion (see Note 10)		9	μs

NOTES: 2. Analog input voltages greater than that applied to REF + convert as all ones (111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+}-V_{ref-}); however, the electrical specifications are no longer applicable.

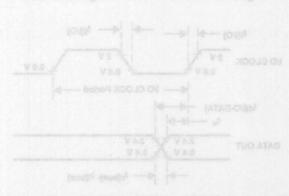
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

7. Zero error is the difference between 000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.

8. Total unadjusted error comprises linearity, zero, and full-scale errors.

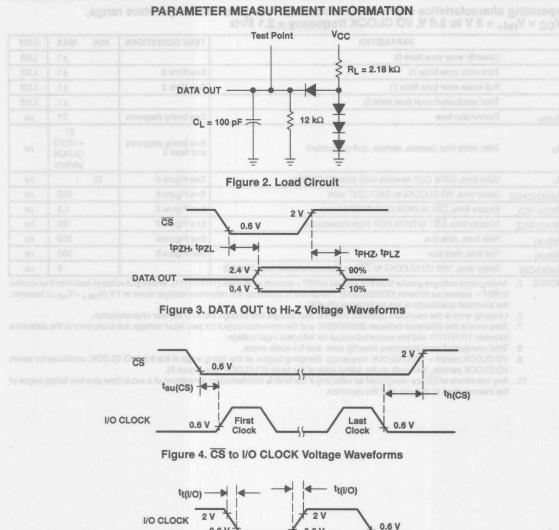
9. I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the tenth I/O CLOCK (see Figure 5).

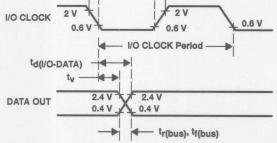
10. Any transitions of CS are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.



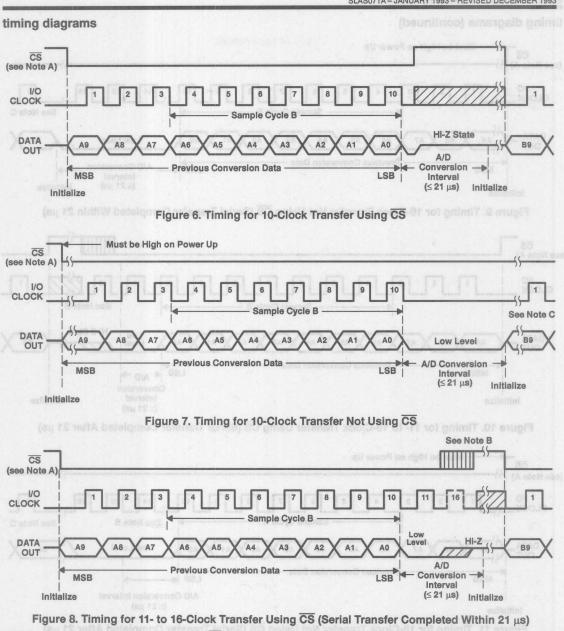


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NOTES: A. To minimize errors caused by noise at \overline{CS} , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum \overline{CS} setup time has elapsed.

- B. A low-to-high transition of CS disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
- C. The first I/O CLOCK must occur after the end of the previous conversion.



TLV1549C 10-BIT ANALOG-TO-DIGITAL CONVERTER WITH SERIAL CONTROL

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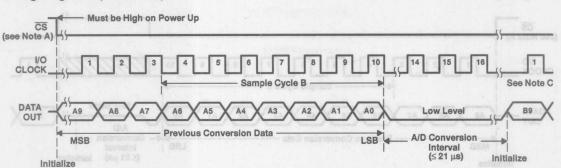


Figure 9. Timing for 16-Clock Transfer Not Using CS (Serial Transfer Completed Within 21 μs)

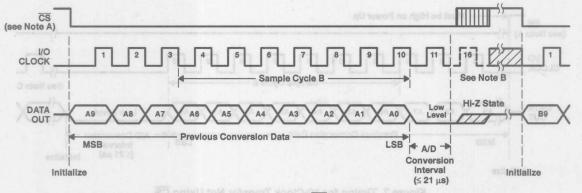


Figure 10. Timing for 11- to 16-Clock Transfer Using CS (Serial Transfer Completed After 21 µs)

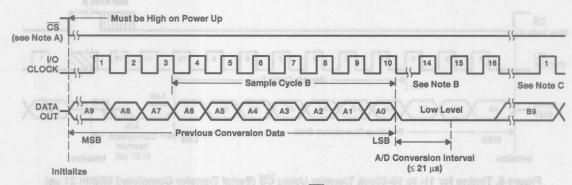


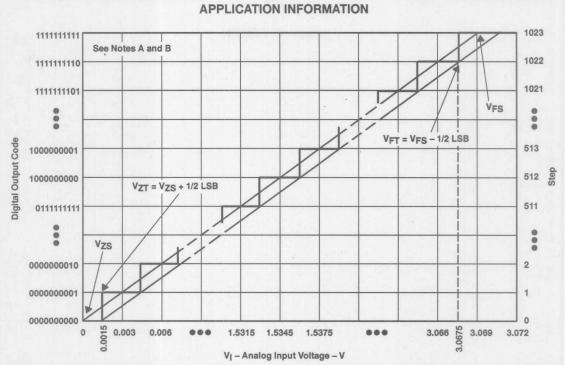
Figure 11. Timing for 16-Clock Transfer Not Using CS (Serial Transfer Completed After 21 µs)

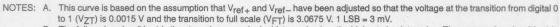
NOTES: A. To minimize errors caused by noise at CS, the internal circuitry waits for a set up time plus two falling edges of the internal system clock after CS↓ before responding to the I/O CLOCK. Therefore, no attempt should be made to clock out the data until the minimum CS setup time has elapsed.

B. A low-to-high transition of CS disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

C. The first I/O CLOCK must occur after the end of the previous conversion.







B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.



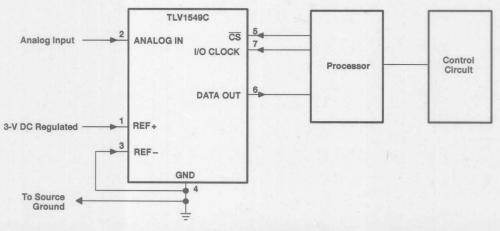
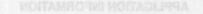


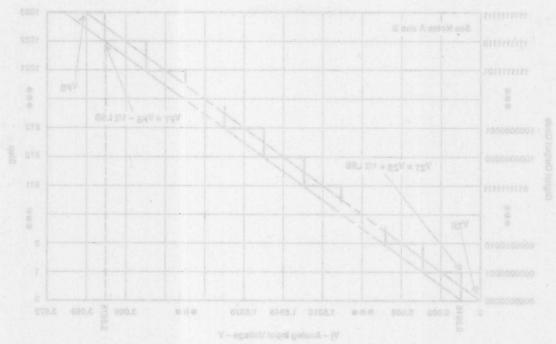
Figure 13. Typical Serial Interface





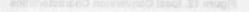
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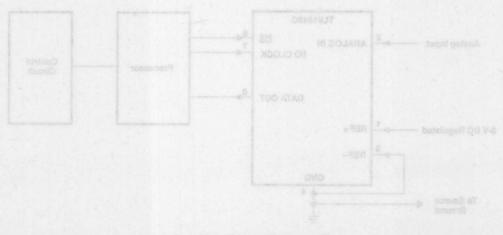




OTES: A. This curve is based on the assumption that V_{REF} and V_{REF} have been adjusted so that the voltage at the transition from digital 0 to 1 (Vyr) is 0.0015 V and the transition from digital 0.

E. The full-scale value (Vpg) is the stap whose nominal midetap value has the highest absolute value. The zero-scale value (Vpg) is the stap whose nominal midstap value equats zero.





Piguna 13, Teploal Sorial Interface

General Information	1
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Voltage Regulators	4
P-Channel MOSFETs	5
Analog-to-Digital Converters	6
Line Driver/Receiver	7
Mechanical Data	8

Comparators	
Analog-to-Digital Converters	

3.3-V MULTICHANNEL RS232 LINE DRIVER/RECEIVER

SLLS135D - FEBRUARY 1992 - REVISED FEBRUARY 1994

- Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Standard RS-232-C)
- Operates With Single 3.3-V Power Supply
- LinBiCMOS[™] Process Technology
- Three Drivers and Five Receivers
- ±30-V Input Levels (Receiver)
- ESD Protection on RS-232 Lines Exceeds 6 kV Per MIL-STD-883C, Method 3015
- Applications
 EIA-232 Interface
 Battery-Powered Systems
 Notebook PC
 Computers
 Terminals
 Modems
- Voltage Converter Operates With Low Capacitance ... 0.47 μF Min

DB PACKAGE (TOP VIEW) VDD 28 C3+ 27 GND C2+[2 Vccl 3 26 C3-25 VSS C2-[] 4 GND 5 24 C1-C1+[23 STBY 6 DIN1 7 22 DOUT1 21 DOUT2 DIN2 8 DIN3 9 20 DOUT3 ROUT1 10 19 RIN1 ROUT2 11 18 RIN2 ROUT3 12 17 RIN3 ROUT4 13 16 RIN4 ROUT5 14 15 RIN5

description

The SN75LV4735[†] is a low-power 3.3-V multichannel RS232 line driver/receiver. It includes three independent RS232 drivers and five independent RS232 receivers. It is designed to operate off a single 3.3-V supply and has an internal switched-capacitor voltage converter to generate the RS232 output levels. The SN75LV4735 provides a single integrated circuit and single 3.3-V supply interface between the asynchronous communications element (ACE or UART) and the serial-port connector of the data terminal equipment (DTE). This device has been designed to conform to standard ANSI/EIA-232-D-1986.

The switched-capacitor voltage converter of the SN75LV4735 uses five small external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 3.3-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept \pm 30 V without damage.

The device also features a reduced power or standby mode that cuts the quiescent power to the integrated circuits when not transmitting data between the CPU and peripheral equipment. The STBY input is driven high for standby (reduced power) mode and driven low for normal operating mode. When in the standby mode, all driver outputs (DOUT1–3) and receiver outputs (ROUT1–5) are in the high-impedance state. If the standby feature is not used in an application, STBY should be tied to GND.

The SN75LV4735 has been designed using LinBiCMOS[™] technology and cells contained in the Texas Instruments LinASIC[™] library. The SN75LV4735 is characterized for operation from 0°C to 70°C.

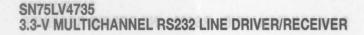
[†] Patent-pending design LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

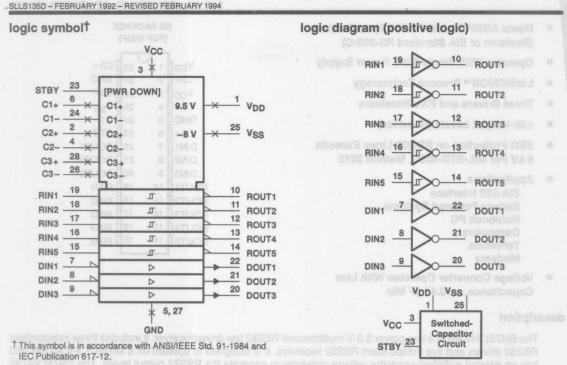
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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a single integrated circuit and single 8.3-V supply interface between the asynchronous mmunications element (AOE or UART) and the serial-port connector of the data terminal equipment (DTE), the device has been designed to conform to standard ANS//EIA-232-D-1988.

The switched-capacitor voltage converter of the SN75LV4735 uses five small external capacitors to generate he positive and negative voltages required by EIA-232 line drivers from a single 3.3-V input. The drivers feature rupput stew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage.

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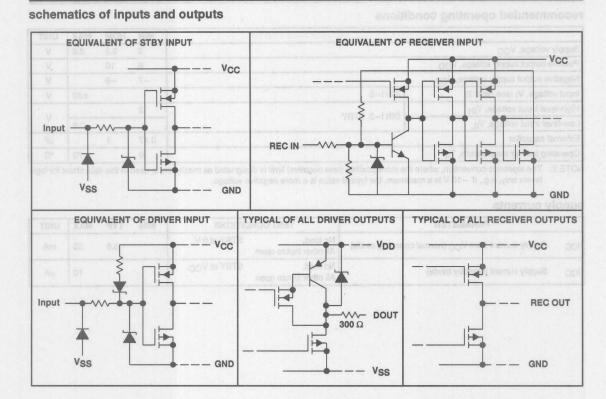
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Negative output supply voltage, V _{SS}	
Input voltage range, V ₁ : DIN1–DIN3, STBY	
RIN1-RIN5	
Output voltage range,Vo: DOUT1-DOUT3 ROUT1-ROUT5	
Continuous total power dissipation	
Operating free-air temperature range, TA	
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: All voltages are with respect to network GND.

DISSIPATION RATING TABLE							
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING				
DB	668 mW	5.3 mW/°C	430 mW				



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recommended operating conditions

chematice of inputs and outputs

Apple and a second s	the men we are a second with the second s	-	MIN	NOM	MAX	UNIT
Supply voltage, VCC						
Positive output supply voltage, VDD	itive output supply voltage, V _{DD}		8	10		V
Negative output supply voltage, VSS	and provide and the ball of the local states o		-7	-8		V
Input voltage, VI (see Note 2)	RIN1–5	1			±30	V
High-level input voltage, VIH	DINH 2 STRV		2			V
Low-level input voltage, VIL	DIN1-3, STB4	DIN1-3, STBY		e-www.	0.8	V
External capacitor	ternal capacitor		0.47	1		μF
Operating free-air temperature, TA		-	0	and the second	70	°C

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

supply currents

	PARAMETER	TEST C	ONDITIONS	MIN	TYP	MAX	UNIT
ICC	Supply current from V _{CC} (normal operatin	g mode) No load, All other inputs op	STBY at 0 V, en		8.5	20	mA
ICC	Supply current (standby mode)	No load, All other inputs op	STBY at V _{CC} , en	En	2	10	μA

absolute maximum ratings over operating free-sir temperature minge (unless otherwise noted)?

Output voltage range, Vo: DOUT1-DOUT3 Vas-0.3 V to VoD + 0.3 V
Operating free-air temperature range, TA

¹ Streams beyond those listed under "stretuin maximum mängst" may cause permanent damage to the device. These are stress ratings only and hubblional operation of this device at these or any other conditions proved those indicated under "recommended operating conditions" is not intolled. Excessure to absolute-maximum-relations for extended periods may effect device reliability. NOTCE 1: All writings are utility memory for each data.



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DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted)

Thette	PARAMETER	PARAMETER				TYPT	MAX	UNIT
VOH	High-level output voltage		$R_L = 3 k\Omega$	aphilov slotis	5.5	7	Whate 9	V
VOL	Low-level output voltage (see Note 2)	Low-level output voltage (see Note 2)				-5.5	Aleyald -	٧
ЧΗ	High-level input current		V _I at V _{CC}	V[T_]	(Vit+=	Risonalisy	1	μA
V	See Note 7 1991 2.4 2.6	STBY	V _I at GND		BELIOV 1	ndano jina	-1	μA
IL V	Low-level input current	Other inputs	V _I at GND		elallov)	udine jev	-10	μA
IOS(H)	High-level short-circuit output current (see No	te 3)	V _{CC} = 3.6 V,	$V_{O} = 0$		-10	-20	mA
IOS(L)	Low-level short-circuit output current (see Not	te 3)	V _{CC} = 3.6 V,	$V_{O} = 0$	isit urix	10	20	mA
ro	Output resistance	$V_{CC} = V_{DD} = V_{S}$ $V_{O} = -2 V \text{ to } 2 V_{S}$		300	iosia	lo gri	Ω	

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

3. Not more than one output should be shorted at one time.

4. Test conditions are those specified by EIA-232-D.

switching characteristics, V_{CC} = 3.3 V \pm 0.3 V, T_A = 0°C to 70°C

121	PARAMETER	TEST CONE	DITIONS	MIN	TYPT	MAX	UNIT
t PLH	Propagation delay time, low-to-high-level output	$R_{\rm L} = 3 \rm k\Omega$ to GND,	CL = 50 pF,	200	400	600	ns
t PHL	Propagation delay time, high-to-low-level output	See Figure 2	VI 632) 10V01 WOI 7	100	200	350	ns
tPZL	Output enable time to low level (see Note 5)	une alterate trate () and a	o v, rg = cb v. son STBV la delva	9.4.001	3	7	ms
^t PZH	Output enable time to high level (see Note 5)	$R_{\rm L} = 3 k\Omega$ to GND,	CL = 50 pF,		1	5	ms
tPHZ	Output disable time from high level (see Note 5)	See Figure 3			1	3	μs
tPLZ	Output disable time from low level (see Note 5)				0.5	3	μs
SR	Output slew rate (see Note 6)	$R_L = 3 k\Omega$ to 7 kΩ, See Figure 2	C _L = 50 pF,	3		30	V/µs
SR(tr)	Transition region slew rate	$R_L = 3 k\Omega$ to GND, See Figure 4	C _L = 2500 pF,		3		V/µs

⁺ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. NOTES: 5. Output enable occurs when STBY is driven low. Output disable occurs when STBY is driven high.

6. Measured between 3-V and -3-V points of output waveform (EIA-232-D conditions); all unused inputs are tied either high or low.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TIMU	PARAMETER	TEST CONDITIONS	MIN	TYPT	MAX	UNIT
VIT+	Positive-going input threshold voltage	(Fig. 1916)	onaflov i	2.2	2.6	V
VIT-	Negative-going input threshold voltage	(See Note 2) 8 10	0.6	heren 1	Low-In	V
Vhys	Input hysteresis (VIT+ - VIT-)	New Yes	0.5	1.2	1.8	V
VOH	High-level output voltage	$I_{OH} = -2 \text{ mA}$, See Note 7	2.4	2.6		V
VOL	Low-level output voltage	IOL = 2 mA	NUT THE	0.2	0.4	V
rj	Input resistance	$V_{I} = \pm 3 V$ to $\pm 25 V$	3	5	7	kΩ

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs remains in the high state.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, CL = 50 pF

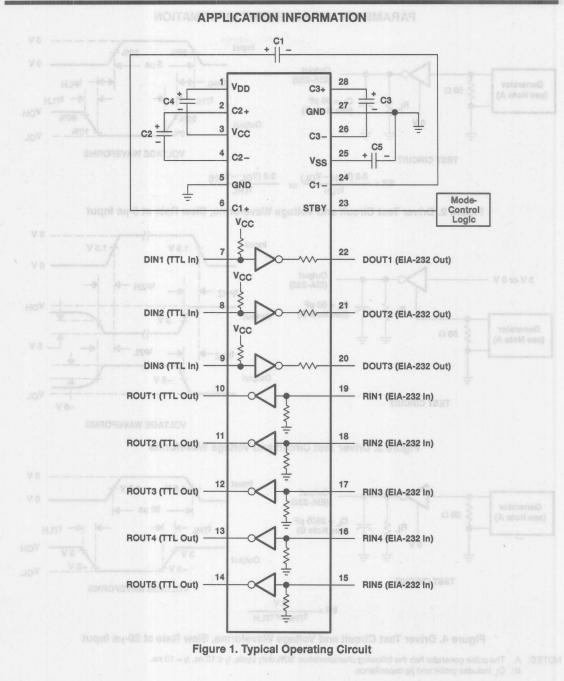
	PARAMETER	TEST CONDITIONS	MIN	TYPT	MAX	UNIT	
tPLH	Propagation delay time, low-to-high-level output	D. 2 KO to CND See Figure 5	45	80	130	ns	
t PHL	Propagation delay time, high-to-low-level output	$R_L = 3 k\Omega$ to GND, See Figure 5	70	100	170	ns	
t _{PZL}	Output enable time to low level (see Note 5)	3. VCC = 3.3 V ± 0.3 V, TA = 07	phalte	160	250	ns	
^t PZH	Output enable time to high level (see Note 5)	D: 2 KO to CND See Figure 6	20.0 80.00	4	10	μs	
t _{PHZ}	Output disable time from high level (see Note 5)	$R_L = 3 k\Omega$ to GND, See Figure 6	arrit wa	300	500	ns	
tPLZ	Output disable time from low level (see Note 5)		and the second s	140	200	ns	

1 All typical values are at V_{CC} = 3.3 V, 1_A = 25°C. NOTE 5: Output enable occurs when STBY is driven low. Output disable occurs when STBY input is driven high.

			RI = 3 karto GND.	
		OL = 2600 pF,		eten welcon region alem rete



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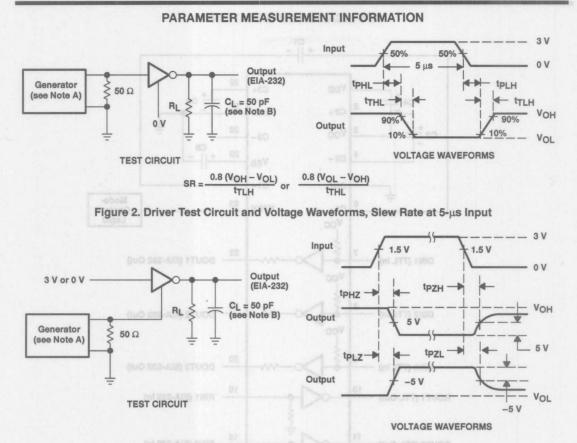
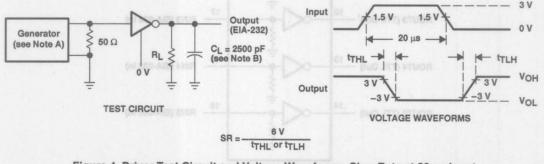


Figure 3. Driver Test Circuit and Voltage Waveforms





- NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_f \le 10$ ns, $t_f = 10$ ns.
 - B. CL includes probe and jig capacitance.



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PARAMETER MEASUREMENT INFORMATION

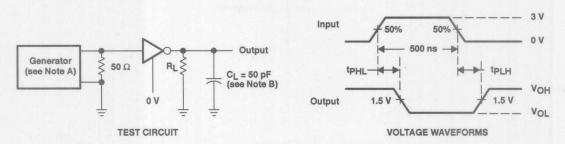
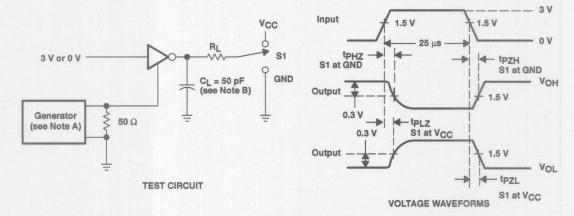


Figure 5. Receiver Test Circuit and Voltage Waveforms



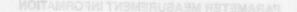
/ Figure 6. Receiver Test Circuit and Voltage Waveforms Enable and Disable Times

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_{f} \le 10$ ns, $t_{f} = 10$ ns. B. CL includes probe and jig capacitance.



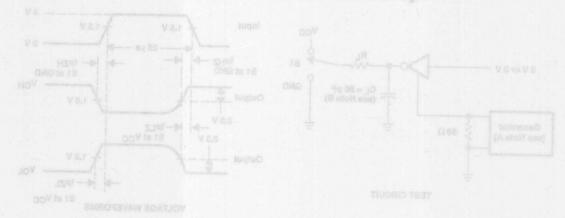


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Floure 5. Receiver Teet Circuit and Voltage Waveforms



Plaure 6. Reseiver Test Orout and Voltage Waveforms Enable and Liseable mess

NOTES: A. The pulse generator has the following characteristics: PRP = 1 MHz, 50% duty cycle, ty 510 ns, ty = 10 ns.

General Information	1
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General Information **Voltage Regulators**

MARCH 1994

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

			Example:	SN	A.	75189		N	-00	
						1		1	(6.20) (8.60) 0.457 (4	
Prefix ———	0.337	0.188	seise a						0.160.0	
MUST CONTA	IN TW	O, THRE	EE, OR FOUR LETTERS			-		-	1	
			unctions or Interface Product			H				
			CE PREFIXES							
LT			Advanced Micro Device Nationa Linear Technolog	y					80 (1,75) 83 (1,35)	
MC N8T	. A		Maxim Integrated Products Motorola Signetics Fairchild/Nationa	a S		ĒŢ				
			10,03,809,8 1,01,709,8 1,01,709,8	0.020 (0.608)				- Connector	0.010 (0,1 0.004 (0,1	
MUST CONTA (From Indiv			EIGHT CHARACTERS eets)							
EBOR-AVEROB3		75	160B C1154 ALS180						0,080 (1,07) 7) (599 2(010	
Package	546			neters).	sillinn) s	in Indive	ens'ano	diniensi vin	AL All Broost	
MUST CONTA	IN ON	E OR TV	VO LETTERS						G. Landa an	
D, DW, FK, J, I (From Pin-Con			ms on Individual Data Sheet)						 d. body am Mold proj 	
Instructions (I	Dash M	No.)		No. Rogel	1					

MUST CONTAIN TWO NUMBERS

-00 No special instructions

-10 Solder-dipped leads (N, package only)

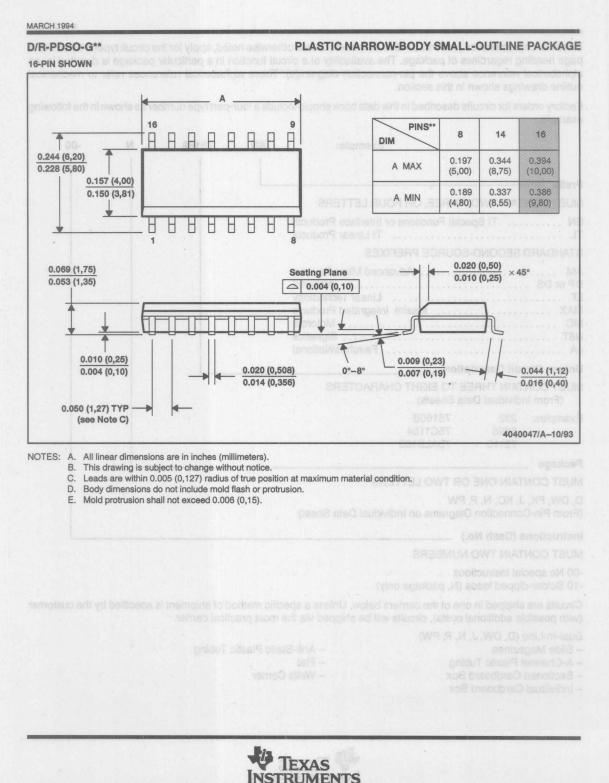
Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (D, DW, J, N, P, PW)

- Slide Magazines
- A-Channel Plastic Tubing
- Sectioned Cardboard Box
- Individual Cardboard Box

- Anti-Static Plastic Tubing
- Flat
- Wells Carrier

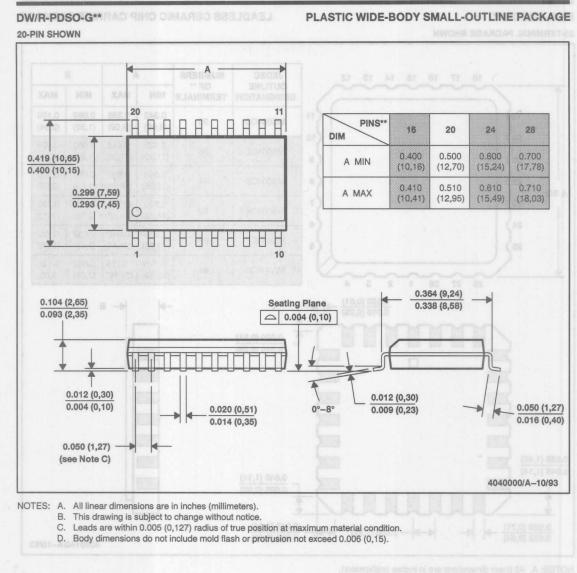




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MARCH 1994



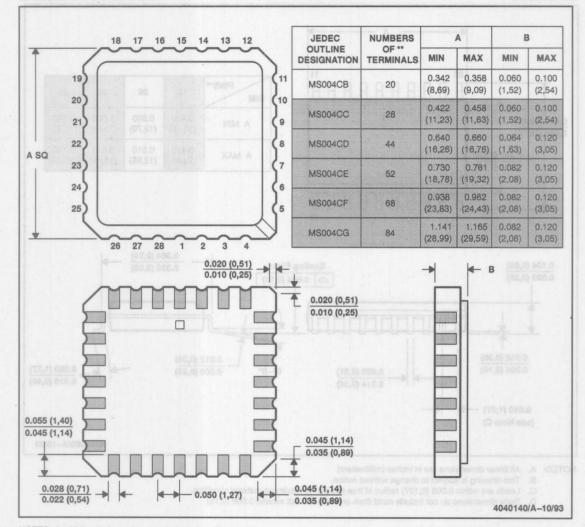


MARCH 1994

FK/S-CQCC-N**

LEADLESS CERAMIC CHIP CARRIER PACKAGE

28-TERMINAL PACKAGE SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals will be gold plated.



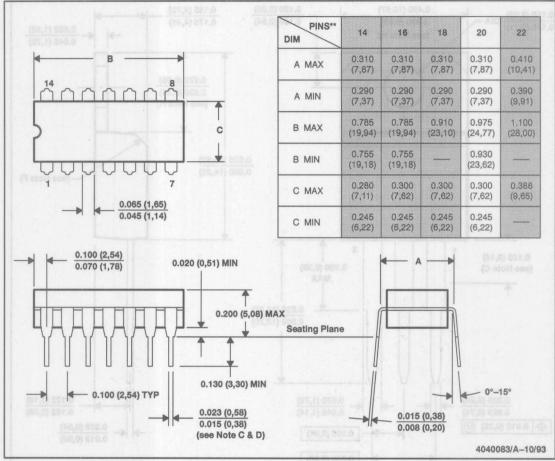
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MARCH 1994

J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14-PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

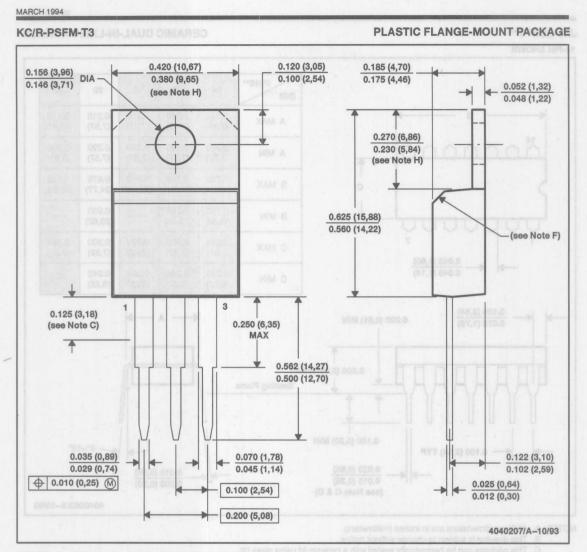
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

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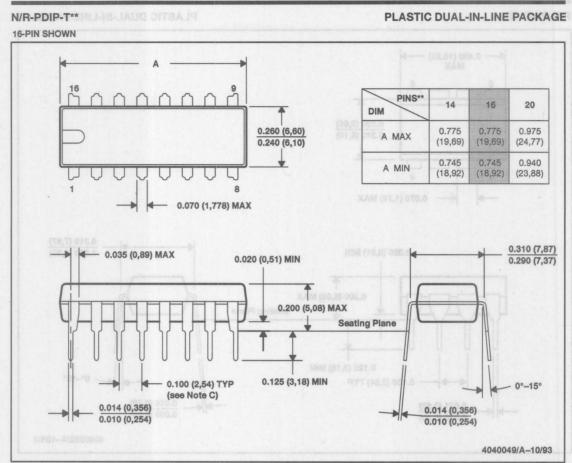


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. Chamfer optional
- G. Falls within JEDEC TO-220AB
- H. Tab contour optional within these dimensions







NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

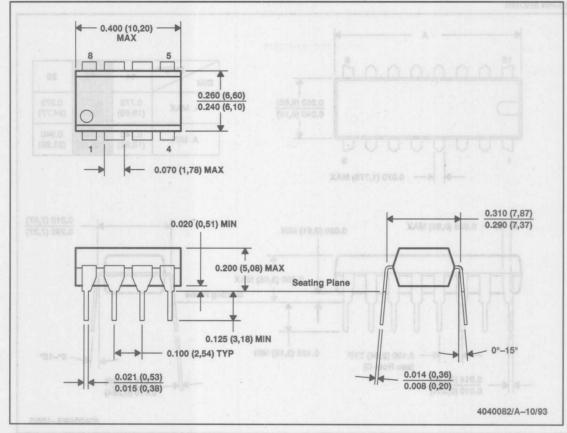
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.





P/R-PDIP-T8

PLASTIC DUAL-IN-LINE PACKAGE

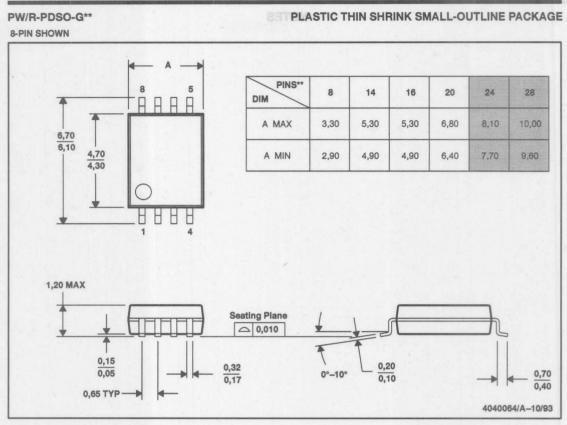


NOTES: A. All linear dimensions are in inches (millimeters). B. This drawing is subject to change without notice.

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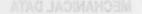
MARCH 1994

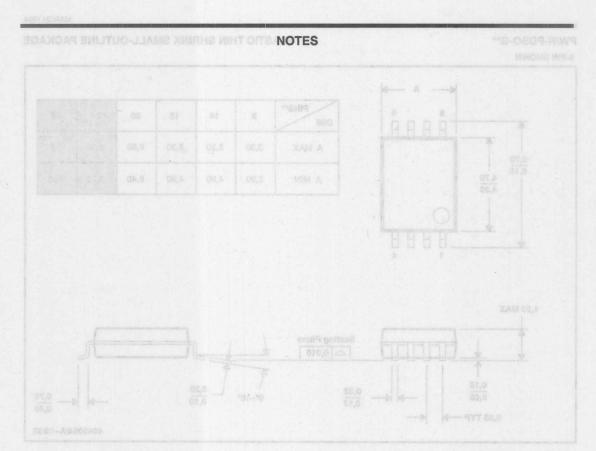


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.
C. Leads are within 0,127 radius of true position at maximum material condition.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.







OTES: A. Althread dimensions are in millimated

If his drawing is subject to change without notice.

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Body dimensions do not initiale most liasts or profigueion, not to expeed 0,15.